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13. ABSTRACT *(Maximum 200 words)*

In this program, we introduced several new concepts which are directed at considerably reducing the complexity of existing optoelectronic integrated circuits (OEICs) and their associated systems by providing 100% of the power requirements of the circuits located at the remote node from the near-end terminal using optical means. In particular, remote powering via the use of monolithically integrated photovoltaic (PV) cells associated with each circuit was demonstrated in the $In_{0.53}Ga_{0.47}As/InP$ materials system. A novel optical logic circuit which could be optically configured to operate variously as an amplifier, bistable switch, latching switch, S-R flip flop or an inverter was used as the focus of this demonstration. Furthermore, very high sensitivity, novel heterojunction phototransistors were demonstrated for use in high sensitivity, low power applications which typify optically powered circuits. It is expected that providing local, "contactless" power using PV cells monolithically integrated onto the functional OEIC chip can be used to advantage in highly complex, high density optical interconnect and optical computing systems. The study of these latter applications was a central feature of a broader program which we are now pursuing at Princeton University.

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CONTACTLESS OPTOELECTRONIC INTEGRATED CIRCUITS FOR REMOTE FIBER OPTIC COMMUNICATION AND SENSING APPLICATIONS

FINAL REPORT

STEPHEN R. FORREST

U.S. ARMY RESEARCH OFFICE

CONTRACT NUMBER DAAL03-89-K-0021

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1.0 Statement of Problem

Numerous fiber optic remote sensing applications place severe restrictions on the photonic devices which perform the actual sensing function. These restrictions concern the speed, size, weight, power dissipation, and sensitivity of the devices which are often placed in adverse environments. Given the availability of the appropriate device structures and functions, however, it is expected that such remote sensing systems will find widespread use in a multitude of applications. To name only a few, these applications include the transceiving of telemetric data to and from terminals located in robotic vehicles where economy of size and space is at a premium, use in heat and pressure sensors located in hostile environments, and the utilization as intravenous probes which can determine the characteristics of, for example, the temperature or gas composition in the bloodstream, etc. In many cases, the distance between the near end terminal and the remote probe is very long (~100 km), thus necessitating the use of long-wavelength (1.3 and 1.55 μm) light coupled into highly transparent optical fibers. In this program, we introduced several new concepts which are directed at considerably reducing the complexity of existing optoelectronic integrated circuits (OEICs) and their associated systems by providing 100% of the power requirements of the circuits located at the remote node from the near-end terminal using optical means. In particular, remote powering via the use of monolithically integrated photovoltaic (PV) cells associated with each circuit was demonstrated in the $In_{0.53}Ga_{0.47}As/InP$ materials system. A novel optical logic circuit which could be optically configured to operate variously as an amplifier, bistable switch, latching switch, S-R flip flop or an inverter was used as the focus of this demonstration. Furthermore, very high sensitivity, novel heterojunction phototransistors were demonstrated for use in high sensitivity, low power applications which typify optically powered circuits. It is expected that providing local, "contactless" power using PV cells monolithically integrated onto the functional OEIC chip can be used to advantage in highly complex, high density optical interconnect and optical computing systems. The study of these latter applications was a central feature of a broader program which we are now pursuing at Princeton University.

2.0 Approaches Used

The program provided novel solutions to many of the various issues concerning remote circuits and devices. In particular, we investigated materials, devices and systems which make use of circuits which require no contacts to the external circuits. The power required to drive the devices was supplied using optical means, whereby a light beam, separate from the beam which carries the data to and from the circuit, is incident on integrated photovoltaic (PV) elements. These elements provided the necessary power to the OEICs, but they also were used in logic circuits to enable or disable a particular gate.

Since the goals of the project were to demonstrate the device concepts in a prototype system, it was necessary to engage in a broad research program which included investigating the semiconductor materials growth processes to ensure material uniformity, developing novel, photovoltaically powered OEIC detection circuits, and implementation of the circuits in prototype demonstration systems. The key results of this program are detailed below:

A. High sensitivity heterojunction phototransistors

To obtain the highest gain at the lowest possible circuit power dissipation, as is required for optically powered circuits (which are inherently "power starved"), we began our investigations by demonstrating a novel heterojunction bipolar transistor technology ideally suited to this application. Thus. a novel, high sensitivity phototransistor for use in very low power circuit applications was demonstrated. This device, known as the high doped, low doped dual emitter (or HILOE) transistor, which has both high bandwidth and good responsivity at low input optical powers, was fabricated using $In_{0.53}Ga_{0.47}As/InP$ due to its compatibility with long wavelength communication as well as its low power requirements. The design of the HILOE structure was optimized using computer solutions to Poisson's Equation developed in our laboratory under a previous ARO contract. Basically, the dual doped emitter greatly reduces carrier recombination at the $In_{0.53}Ga_{0.47}As/InP$ heterojunction, thereby increasing transistor gain at low base currents (and hence low input optical powers).

A comparison of HILOE and conventional phototransistor gain as a function of collector current is shown in Fig. 1. Here, the gain of the HILOE device is clearly superior at low values of collector current, I_C, corresponding to

weak optical input signals (i.e.; small base current, I_B). Record high gains at powers of as low as 40 nW were observed, and were successfully modelled using a computer solution to Poisson's Equation. The f_T for the device is 10–20 GHz, which makes it an outstanding candidate for high bandwidth, high sensitivity integrated photoreceivers. This is particularly true since the phototransistor is easily integrated with a bipolar transistor preamplifier.

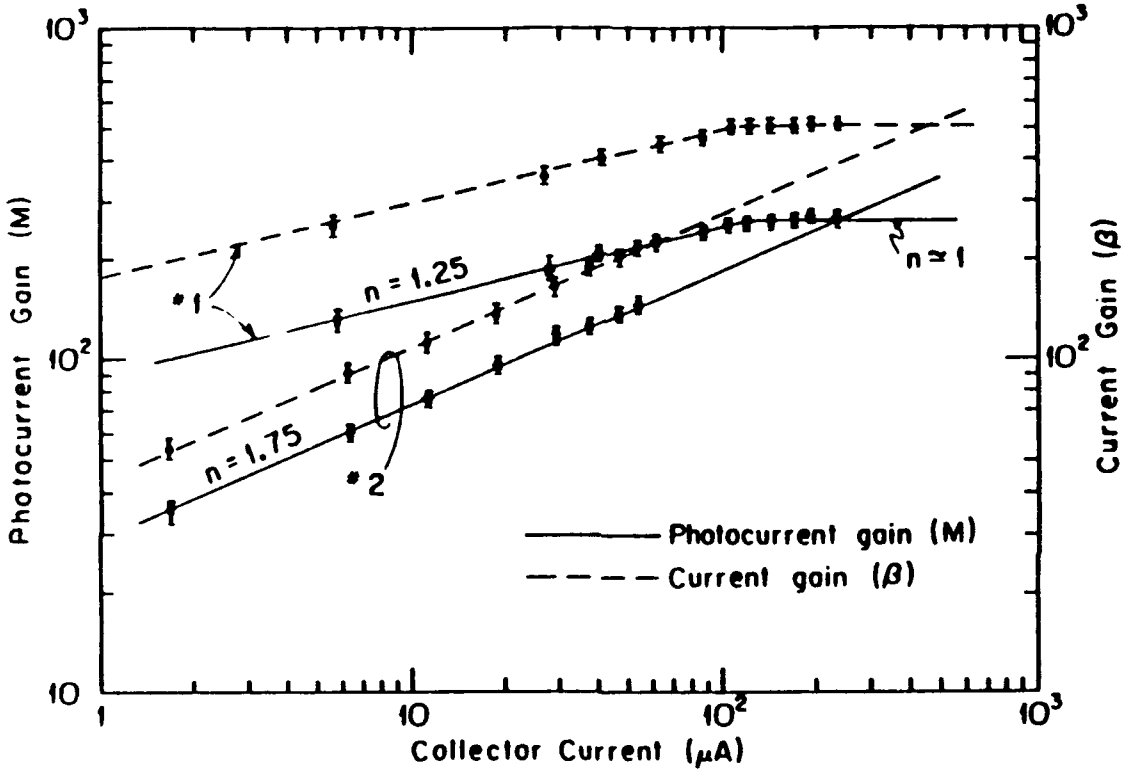

Fig. 1: Comparison of the collector characteristics of a HILOE and a conventional heterojunction phototransistor. Note the high gain at low I_C.

B. Integration of optical logic

As the demonstration, optically powered device, we integrated a unique optoelectronic logic "transceiver" in the $In_{0.53}Ga_{0.47}As/InP$ based materials system whose circuit is shown in Fig. 2. Full operation of the optical logic elements was then demonstrated under optical powering. That is, the fully integrated optical logic circuit with two HPTs for optical input and feedback, an HBT for laser prebias, a photoconductor (PC) for feedback control, a PC for reset and a series resistor for output clamping all worked together using a PV cell array to supply power to the circuit. This is perhaps a demonstration of the most complex InP-based OEIC (from a device diversity standpoint)

demonstrated to date. The circuit exhibited amplification, bistability, latching, invert, and set-reset flip-flop modes of operation with varying levels of feedback power (P_{fb}) incident on the feedback PC. The transfer function of the switch is shown in Fig. 3. The first generation circuit had an optoelectronic gain (P_{out}/P_{in}) of 2.5 to 11, a bandwidth of 40 MHz, and a switching energy of only 3.8 pJ. These results are extremely encouraging since they point to excellent performance in subsequent iterations of the same circuit (i.e., no fundamental design changes) by simply increasing the HPT gain, which was somewhat low for the present circuit (50) due to a wide base region. Switching energies as low as 50 fJ are therefore expected once the growth technology used is improved to obtain thinner base widths. This is the best performance anticipated for an optoelectronic switch of any kind.

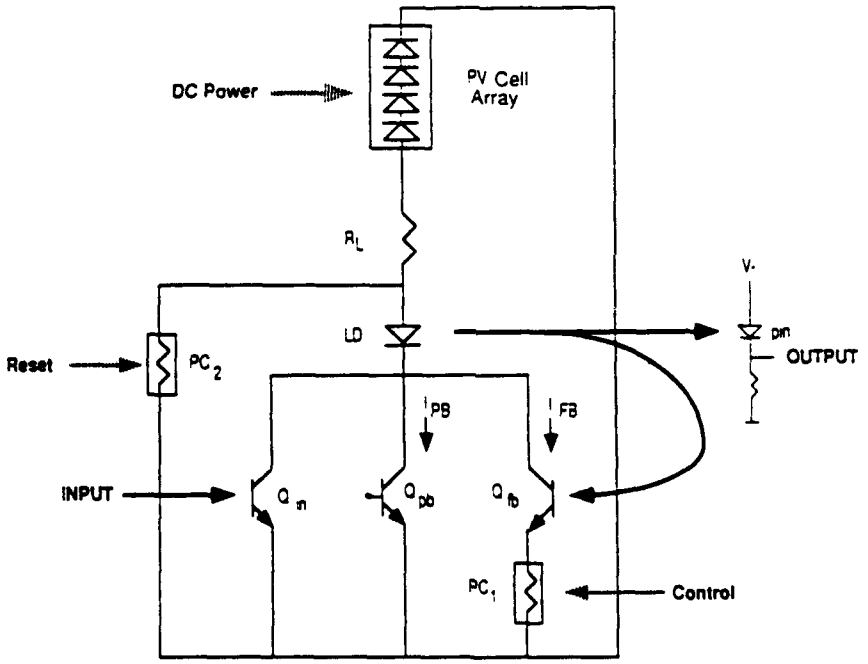

Fig. 2: Schematic diagram of the integrated optoelectronic logic circuit.

A summary of the circuit performance is given in the table below. The column listed as "Expected" assumes only modest improvements in the existing circuit performance. That is, the circuit, as designed, should perform to this level when all of the devices on board are optimized.

Table 1
Optical Logic Circuit Performance

Parameter	Meas.	Expected
Gain (P_{out}/P_{in})	2.5 – 11	50
Bandwidth (MHz)	40	500
Power Dissipation (mW)	5.3	2
Contrast Ratio	>100	>100
Switching Energy (pJ)	3.8	0.05
Pixel Density (#/cm^2)	300	500

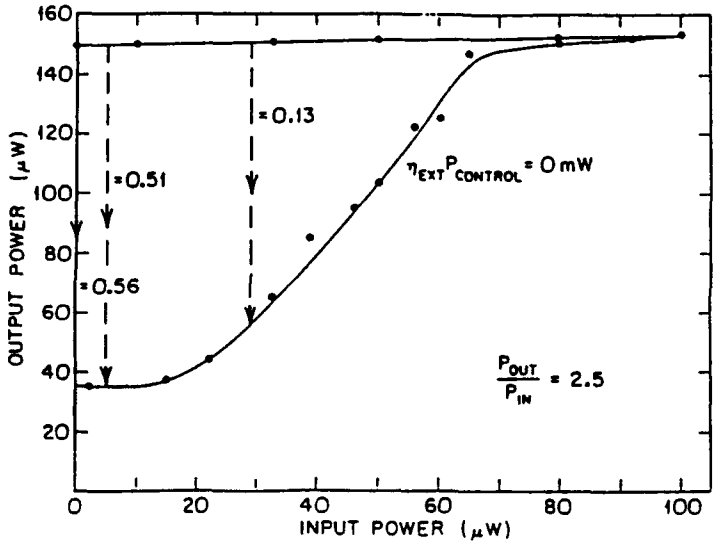

Fig 3: Transfer function of the circuit shown in Fig. 2 using various control current intensities.

C. Two-sided wafer growth

A key technology for making optically powered OEICs efficiently coupled to optical fibers is two-sided wafer growth. As shown in earlier work by Govindarajan and Forrest (Applied Optics, April 10, 1991), growth of the PV cell on the wafer surface opposite that of the data detection circuitry greatly reduces cross-talk between the power and data channels. That is, the intervening InP substrate efficiently isolates the devices on the opposite wafer surfaces from optical cross-talk. Thus, we also performed work on growing epitaxial layers on both wafer surfaces. In these experiments, we concentrated on growing an HPT

structure on one wafer surface, and then subsequently growing a single, undoped InP layer on the opposite wafer surface which is used as the PV cell absorbing layer. Between growths, the HPT layers are coated with an encapsulating SiN_x layer which prevents surface decomposition during the second growth sequence. Here, the SiN_x was deposited at 350 °C to a thickness of 1000 Å, and had a SiH_4/N_2 gas composition which results in an index of 2.145 (i.e., the nitride is Si-rich). With this process, the SiN_x as well as the first grown surface withstood the 660 °C second growth. No decomposition of this structure is observed. Only slight "orange peel" texture characteristic of LPE growth is apparent. The doping and thicknesses of the HPT layers are as follows:

Table 2

Material	**Function**	**Doping**	**Thickness**
InGaAs	Collector (n)	$2x10^{17}$	1.0 μm
InGaAs	Base (p)	$7x10^{18}$	0.2 μm
InP	Emitter (n)	$7x10^{17}$	1.5 μm

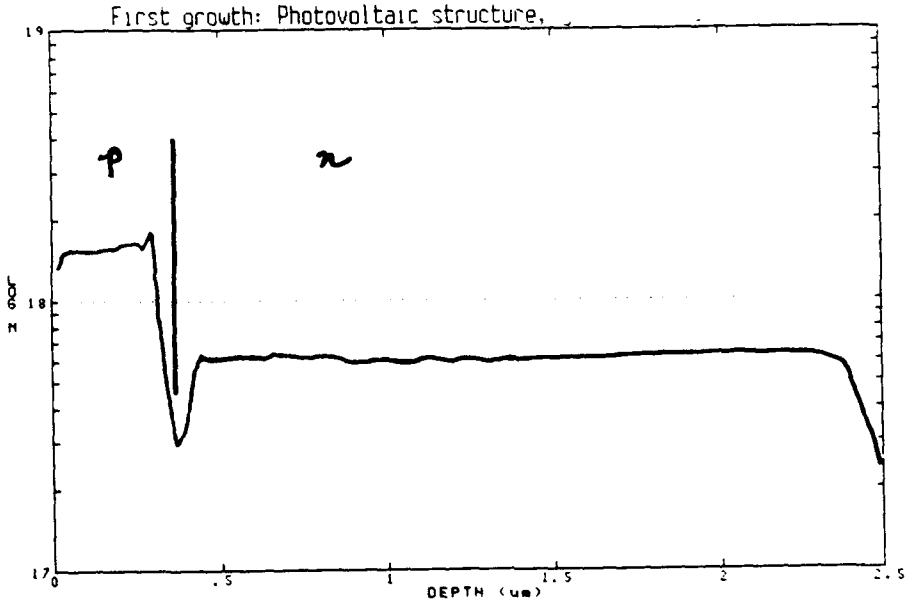

Fig. 4a: Polaron plot of the doping and thicknesses of the HBT layers of the two-sided grown wafer.

The doping of each layer (with the exception of the Cd-doped base) is quite uniform, as shown in Fig. 4a. For a typical PV cell, the InP absorbing layer was 2.0 μm thick, and had a uniform background doping of $5x10^{17}$ cm^{-3}. This was capped with a p-InGaAs contact layer, with a doping of 1.5x1018 cm^{-3}. The PV cell layer dopings and thicknesses are shown in Fig. 4b. These results indicate that two-sided wafer growth has been successfully achieved.

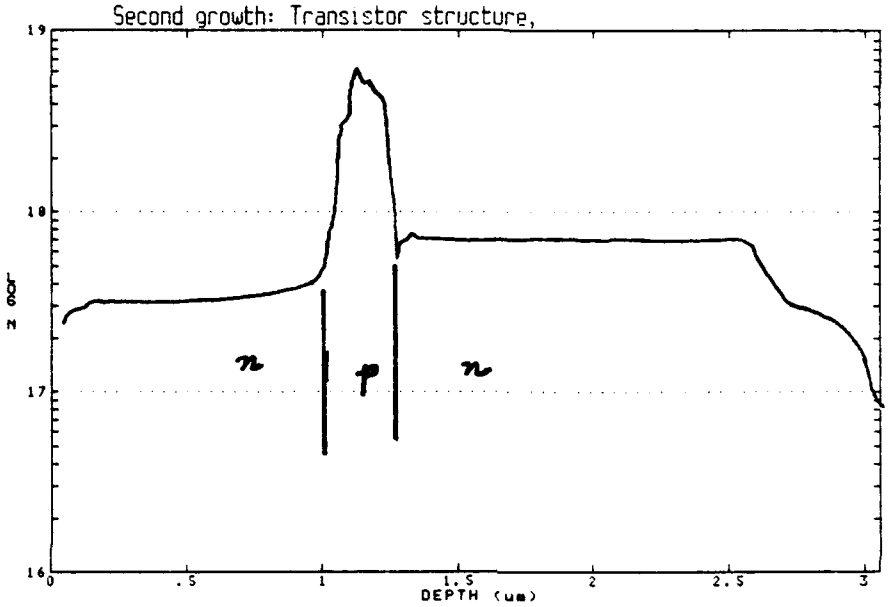

Fig. 4b: Polaron plot of the doping and thicknesses of the PV cell layers of the two-sided grown wafer.

3.0 Publication List

1. "The Effects of Lattice Mismatch on $In_{0.53}Ga_{0.47}As/InP$ Heterojunctions," C. D. Lee and S. R. Forrest, *Appl. Phys. Lett.*, 57, 469 (1990)
2. "A High Sensitivity $In_{0.53}Ga_{0.47}As/InP$ Heterojunction Phototransistor," L. Y Leu, J. T. Gardner and S. R. Forrest, *Appl. Phys. Lett.*, 57, 1251 (1990)
3. "A High Gain, High Bandwidth $In_{0.53}Ga_{0.47}As/InP$ Heterojunction Phototransistor for Optical Communications," L. Y. Leu, J. T. Gardner and S. R. Forrest, *J. Appl. Phys.*, 69, 1052 (1990)
4. "$In_{0.53}Ga_{0.47}As/InP$ Heterojunctions with Low Interface Defect Densities," C. D. Lee and S. R. Forrest, *J. Appl. Phys.*, 69, 342 (1990)
5. "Optically Powered Optoelectronic Interconnection Arrays," M. Govindarajan and S. R. Forrest, *Applied Optics*, 30, 1335 (1990)
6. "Optically Powered Arrays for Optoelectronic Interconnection Networks," M. Govindarajan and S. R. Forrest, *GOMAC '90*, Las Vegas, NV (Nov., 1990)
7. "A High Sensitivity, High Bandwidth $In_{0.53}Ga_{0.47}As/InP$ Heterojunction Phototransistor," L. Leu, J. Gardner and S. R. Forrest, *Integrated Electronic Devices Meeting*, Paper 6.7, San Francisco, CA (Dec. 9–12, 1990)
8. "Optically Powered Monolithically Integrated Optical Logic Circuits," J. J. Brown, J. T. Gardner and S. R. Forrest, *Integrated Photonics Research Conf.*, Monterey, CA (April, 1991)
9. Optically Powered Smart Pixels," S. R. Forrest, J. J. Brown, J. Gardner, (invited paper) *Optical Society of America Annual Meeting*, San Jose, CA (1991)

4.0 Participating Personnel

1. Len-Yi Leu: PhD awarded, USC, December, 1990.
2. Chia-Di Lee: PhD awarded, USC, April, 1991
3. James T. Gardner, PhD anticipated, USC, January, 1993

5.0 Inventions

None

6.0 Appendices: Reprints of Publications Acknowledging ARO Support

A. "The Effects of Lattice Mismatch on $In_{0.53}Ga_{0.47}As$/InP Heterojunctions," C. D. Lee and S. R. Forrest, *Appl. Phys. Lett.*, 57, 469 (1990)

B. "A High Sensitivity $In_{0.53}Ga_{0.47}As$/InP Heterojunction Phototransistor," L. Y Leu, J. T. Gardner and S. R. Forrest, *Appl. Phys. Lett.*, 57, 1251 (1990)

C. "A High Gain, High Bandwidth $In_{0.53}Ga_{0.47}As$/InP Heterojunction Phototransistor for Optical Communications," L. Y. Leu, J. T. Gardner and S. R. Forrest, *J. Appl. Phys.*, 69, 1052 (1990)

D. "$In_{0.53}Ga_{0.47}As$/InP Heterojunctions with Low Interface Defect Densities," C. D. Lee and S. R. Forrest, *J. Appl. Phys.*, 69, 342 (1990)

E. "Optically Powered Optoelectronic Interconnection Arrays," M. Govindarajan and S. R. Forrest, *Applied Optics*, 30, 1335 (1990)

F. "A High Sensitivity, High Bandwidth $In_{0.53}Ga_{0.47}As$/InP Heterojunction Phototransistor," L. Leu, J. Gardner and S. R. Forrest, *Int. Electron Devices Meeting*, Paper 6.7, San Francisco, CA (Dec. 9–12, 1990)

G. "Optically Powered Monolithically Integrated Optical Logic Circuits," J. J. Brown, J. T. Gardner and S. R. Forrest, *Integrated Photonics Research Conf.*, Monterey, CA (April, 1991)

H. Optically Powered Smart Pixels," S. R. Forrest, J. J. Brown, J. Gardner, (invited paper) *Optical Society of America Annual Meeting*, San Jose, CA (1991)

A. Effects of lattice mismatch on $In_xGa_{1-x}As/InP$ heterojunctions

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The conduction-band discontinuities and interface charge densities of several *n-N* isotype $In_xGa_{1-x}As/InP$ ($x \simeq 0.53$) heterojunctions with lattice mismatches ($\Delta a/a$) ranging from $+0.26$ to -0.24% were measured using capacitance-voltage techniques. To facilitate these measurements, organic-on-inorganic contact barrier diodes were used. Extremely low interface charge densities ($< 1\times10^{10}$ cm^{-2}) are obtained for all the samples, which are approximately one order of magnitude lower than previously reported values for these heterojunctions. We find that the interface charge density is independent of the magnitude of lattice mismatch and temperature. All the samples show a clear peak-and-notch in their apparent free-carrier concentration profiles at temperatures as low as 83 K. This is in contrast to results reported previously where the notch is observed to disappear at low temperature. The measured heterojunction conduction-band discontinuity is also found to be temperature independent, with a value of 0.22 ± 0.02 eV.

It is well known that defects at heterojunctions can affect the performance of optoelectronic devices. For example, lattice mismatch induced dark-line defects at AlGaAs/GaAs heterojunctions are known to be a principle source of laser degradation.[1] In heterojunction (HJ) systems such as InGaAs(P)/InP where there is no "natural" lattice match condition, great care must be taken during growth to ensure that the composition of the quaternary semiconductor gives a near perfect lattice match. If such a condition is not met, a large number of defects can be generated which propagate from the heterointerface. Other researchers[2,3] have speculated that this lattice mismatch in InGaAs(P)/InP HJs results in a very high density of localized defect charge. The presence of the charge is inferred from a severe distortion in the free-carrier concentration profiles of these HJs obtained at low temperature[2,3] using capacitance-voltage (C-V) techniques.[4] To date, however, there has been no systematic study which indicates that this fixed charge, which has been universally observed in $In_{0.53}Ga_{0.47}As/InP$ HJs, is in fact due to lattice mismatch.

In this study, we have grown a series of $In_xGa_{1-x}As/InP$ heterojunctions in which the lattice mismatch was varied over a very broad range; i.e., from -0.24 to $+0.26\%$. Here, positive mismatch corresponds to compositions of $In_xGa_{1-x}As$ whose lattice constant is larger than that of InP. Using C-V techniques, we find that there is no correlation between lattice mismatch and fixed interface charge density. Furthermore, the charge densities measured in our samples are significantly lower than 10^{10} cm^{-2}, which to our knowledge represent the lowest values yet reported for $In_{0.53}Ga_{0.47}As/InP$ HJs. We observe, for the first time, that the free-carrier concentration profile measured in the heterointerface region is temperature independent, indicative of the high quality of the HJs studied. From these results, we conclude that the source of the widely observed temperature dependence of these profiles is a result of native defects or impurities introduced during growth, which are noticeably absent in our growth process.

As noted above, a good measure of the heterointerface quality is the density of the fixed charges which reside at the heterointerface. The dangling bonds and defects caused by the lattice mismatch, *if* they are electrically active, should trap free carriers and create fixed interface charges. Kroemer *et al.*[4] have shown that the conduction-band discontinuity and interface charge density can be determined from the apparent free-carrier concentration profiles obtained from C-V measurements. The band diagram of an *n-N* isotype type 1 heterojunction, such as $In_{0.53}Ga_{0.47}As/InP$, is shown in the inset of Fig. 1. From this diagram, it is apparent that the conduction-band offset energy is related to the diffusion potential V_D across the heterojunction via

$$\Delta E_c = qV_D + \delta_1 - \delta_2. \tag{1}$$

Here, q is the electronic charge, and δ_1 and δ_2 are the depths of the Fermi levels as measured from the conduction-band edges in the large and small band-gap layers, respectively. The diffusion potential across the heterojunction, V_D, is given by[4]

$$V_D = \frac{q}{\epsilon}\int_{-\infty}^{\infty} [N_d(x^*) - n(x^*)](x^* - x_j)dx^*. \tag{2}$$

The fixed charge density at the heterojunction, σ, is determined using

$$\sigma = \int_0^{\infty} [N_d(x^*) - n^*(x^*)]dx^*, \tag{3}$$

where ϵ is the semiconductor permittivity, and $n^*(x^*)$ is the measured apparent free-carrier concentration determined using standard C-V analysis methods.[5] Also, $N_d(x^*)$ is the background doping concentration which is equal to $n^*(x^*)$ in the InP and $In_{0.53}Ga_{0.47}As$ layers far away from the heterojunction, and x_j is the actual distance of the heterojunction from the rectifying contact.

Three liquid phase epitaxially (LPE) grown samples have been studied in this experiment. Double-crystal x-ray diffraction was used to determine the lattice mismatch between the $In_xGa_{1-x}As$ layer ($x \simeq 0.53$) and the underlying InP layer. The lattice mismatches of these three samples

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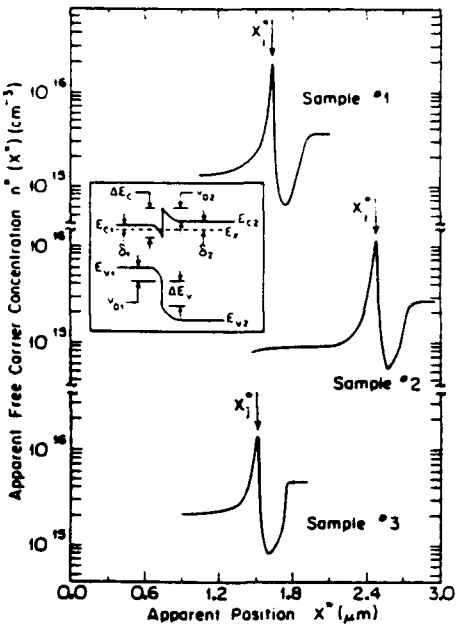

FIG. 1. Apparent free-carrier concentration profiles for sample Nos. 1, 2, and 3 measured at 83 K. The inset shows the energy-band diagram of a typical *n-N* type 1 heterojunction.

are -0.24, -0.03, and $+0.26\%$, corresponding to sample Nos. 1, 2, and 3, respectively. The variation of lattice mismatch across a $(15\ \text{mm})^2$ wafer was found to be less than $\pm 0.03\%$, for the worst case sample.

The InP and $In_xGa_{1-x}As$ layers were grown on (100) S-doped n^+-InP substrates with an electron concentration of approximately $3\times10^{18}\ \text{cm}^{-3}$. Prior to growth, the substrates were organic solvent cleaned, etched in a solution of 3:1:1 H_2SO_4:H_2O_2:H_2O for 4 min, and finally rinsed in de-ionized water immediately before loading into a graphite boat. For surface preservation during heat-up and melt homogenization, the substrate was kept under a Sn-InP melt[6] using a basket inserted into the graphite boat. The growth melt for the $In_xGa_{1-x}As$ layer was prepared using ultrahigh purity $(99.99999+\%)$[7] In prebaked for 24 h at 700 °C. After the bake, 99.9999% pure polycrystalline InAs and GaAs were added to the melt. Lattice mismatch was achieved by varying the percentage of Ga in the melt. We grew seven wafers with different lattice mismatches, and found that the lattice mismatch was almost linearly related to the atomic percentage of Ga in the melt. For a melt liquidus temperature of 650 °C, as X'_{Ga} is changed from 2.51 to 2.30%, the lattice mismatch $(\Delta a/a)$ varied from -0.24 to $+0.26\%$. Here, X'_{Ga} is defined as the atomic percentage of Ga in the melt. The growth solutions were baked prior to growth for 48 h at a temperature 20 °C higher than the liquidus temperature to reduce the background doping concentrations of the layers. The In-InP melt was prepared using prebaked, $99.99999+\%$ In. The melt was then baked for an additional 48 h after adding a small amount of InP for saturation purposes. The substrate was slid through an undersaturated In-InP melt just before growth to obtain a fresh surface.

A 2–3-μm-thick InP buffer layer was grown by the two-phase method[8] at a rate of 0.3 μm/°C, followed by an $In_xGa_{1-x}As$ layer grown with 3 °C of supercooling at 647 °C. The growth rate of the $In_xGa_{1-x}As$ layer strongly depends on the sign and magnitude of the lattice mismatch, varying from 0.6 μm/°C for $\Delta a/a = +0.26\%$, to 2.1 μm/°C for $\Delta a/a = -0.24\%$. This result is expected since the growth rate is limited by the diffusion of Ga within the melt. To obtain a uniform layer thickness and smooth surface morphology, the furnace was calibrated to obtain a uniform temperature profile to within ± 0.1 °C over a 25 cm length. We found that the surface morphology of negatively lattice-mismatched $In_xGa_{1-x}As$ layers are generally better than those of positively lattice-mismatched ones. In addition, the growth melt cannot be wiped off from the wafer surface for $In_xGa_{1-x}As$ layers with $|\Delta a/a| > 0.3\%$.

To facilitate the *C-V* measurement, organic-on-inorganic (OI) semiconductor contact-barrier diodes were fabricated to form a rectifying contact with the top semiconductor layer.[9,10] These diodes were made in the following manner: A 100 Å Cr followed by a 2000 Å Au layer was vacuum deposited to form the contact on the substrate surface. Next, a 1000-Å-thick layer of the prepurified organic semiconductor was vacuum sublimed onto the epitaxial layer surface of the wafer. The organic compound employed was 3, 4, 9, 10 perylenetetracarboxylic dianhydride (PTCDA). Finally, $5.3\times10^{-4}\ \text{cm}^2$ circular In contacts were deposited onto the PTCDA surface through a shadow mask. The organic layer forms a rectifying HJ barrier with the underlying semiconductor such that large reverse bias voltages can be applied to the diode (typically 18 V for $In_xGa_{1-x}As$ with a doping of $1\times10^{15}\ \text{cm}^{-3}$) without inducing large reverse leakage currents. Usually, the reverse saturation current is less than 10 mA/cm^2, and the sample under study can be deeply depleted prior to undergoing breakdown. A detailed description of the technique of using organic films for wafer analysis is presented elsewhere.[9,10]

Capacitance-voltage measurements were performed at temperatures ranging from 293 to 83 K. The measurement frequency used was 1 MHz, and the ac test signal amplitude was 10 mV_{rms}. The apparent free-carrier concentration profiles of sample Nos. 1, 2, and 3 measured at 83 K are shown in Fig. 1. As shown in this figure, the peak and notch are clearly evident for all three samples, and no distortion of these profiles from room to low temperature are observed. This result contradicts that of Lang *et al.*[11] who suggested that HJ series resistance causes the notch in the $In_{0.53}Ga_{0.47}As$/InP HJs to vanish at low temperature. By that assumption, this distortion should be observed in all low-temperature *C-V* measurements made on this HJ system, in clear contradiction to our results.

The low and flat free-carrier concentrations on both sides of the HJ observed in the profiles in Fig. 1 provide an accurate determination of the background doping concentration (N_d). This minimizes the error in calculating the diffusion potential V_D and conduction-band offset energy ΔE_c using Eqs. (1) and (2). Figure 2 shows the *measured* conduction-band offset energies of these three samples as a function of temperature. As expected, the measured

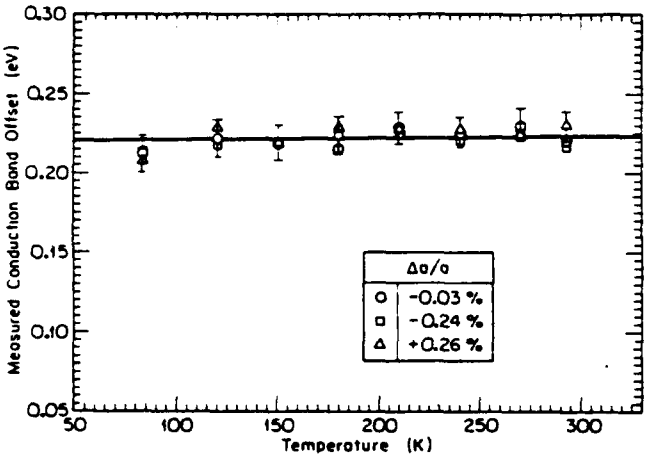

FIG. 2. Measured conduction-band offset as a function of temperature for sample Nos. 1, 2, and 3.

conduction-band offset is independent of temperature, and has an average value of 0.22 ± 0.02 eV. The error bars in the figure are due to the uncertainties in choosing the background doping (N_d) on the $In_xGa_{1-x}As$ side of the heterojunction. This measured band offset value is consistent with previous reports of ΔE_c for $In_{0.53}Ga_{0.47}As/InP$ HJs measured at room temperature.[2,3,11-13] However, to our knowledge, this is the first time that such a value is found to be completely temperature independent, even though in some cases the lattice mismatch is quite large.

The fixed charge density at the heterointerface is shown in Fig. 3 as a function of temperature. The error bars here are also due to uncertainties in determining N_d. Although there is a small variation in σ at different temperatures, the value of σ is at least one order of magnitude smaller than the values reported previously for $In_{0.53}Ga_{0.47}As/InP$ HJs.[2,3,12,13] Since the value of σ is so small, the variation in σ with temperature can be attributed to the limitation on capacitance measurement accuracy. The small σ values in our samples also confirm that the filling in of the notch region in previously reported data[2,3,12,13] is due to charge trapping at a high density of

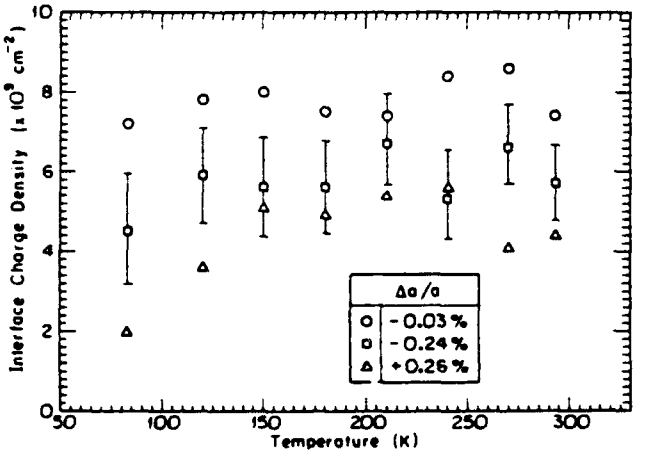

FIG. 3. Interface fixed charge density as a function of temperature for the three samples in Fig. 2.

defects at the heterointerface at low temperature. It is surprising that sample No. 2, which is lattice matched at the growth temperature, has the highest value of σ, whereas sample No. 3, which has $\Delta a/a = +0.26\%$, has the smallest σ. Thus, we can conclude that lattice mismatch has no effect on creating the heterointerface fixed charge. That is, the defects induced by lattice mismatch are not electrically active. The energy states created by defects at the heterointerface are either pulled into the conduction or valence band at the heterointerface, instead of residing in the bandgap region.

In conclusion, we have measured the interface fixed charge density and conduction-band discontinuity of three $In_xGa_{1-x}As/InP$ HJs with lattice mismatches ranging from -0.24 to $+0.26\%$. The measurements show that the interface charge density is independent of both the magnitude and the sign of the lattice mismatch, contrary to assertions made in previous work. We conclude that the fixed interface charges, therefore, must come from the other sources, e.g., from phosphorus vacancies created during wafer translation,[12] or impurities incorporated during growth. In fact, we attribute the very low interface charge densities obtained in this work to the use of ultrahigh purity In in the growth melt. Experiments in our laboratory with slightly less pure In sources (99.99995%) show higher values of σ than those reported here, and a detailed report of those experiments will appear elsewhere. The results described here, therefore, suggest that perfect lattice match is not a strict requirement for devices utilizing this heterojunction system.

From the device processing point of view, slightly negative lattice-mismatched LPE-grown $In_{0.53}Ga_{0.47}As$ might be more suitable for device processing since the surface is smoother than those with perfect or positively mismatched layers. However, for devices requiring thin epitaxial layers, positive lattice mismatch is desired because the growth rate is much slower, and thus the layer thickness is easier to control.

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B. High sensitivity $In_{0.53}Ga_{0.47}As/InP$ heterojunction phototransistor

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We describe both theoretical and experimental investigations of the effects of inserting a thin, low-doped layer into the emitter of an $InP/In_{0.53}Ga_{0.47}As$ heterojunction phototransistor (HPT). This high-low emitter structure has improved sensitivity over conventional structures at low input optical power by decreasing the bulk recombination current at the heterointerface. Experimental data show that the photocurrent gain is independent of the incident optical power at high input powers, corresponding to a heterojunction ideality factor of 1. At low input power, the gain is found to have a small power dependence, with an ideality factor of 1.25. A current gain as high as 260 is obtained at an input power of only 40 nW. These results, which are consistent with numerical simulations of the HPTs, give direct evidence that bulk recombination in the space-charge region at the emitter/base junction is the major source of recombination current for an $InP/In_{0.53}Ga_{0.47}As$ HPT.

It is well known[1] that the photocurrent gain[2] of a typical heterojunction phototransistor (HPT) drops dramatically at low optical power, thereby limiting the sensitivity of the device. This behavior is attributed to different sources of recombination currents, such as Shockley–Read–Hall (SRH) recombination through deep levels, band-to-band radiative, Auger, and surface recombination currents. The understanding of the contribution of each component to the total recombination current, and the suppression of the major recombination source, therefore, are key to the improvement of the sensitivity of HPTs.

Under normal HPT operating conditions, the emitter/base (E/B) junction is forward biased, and most of the recombination current occurs in the space-charge region (SCR) of this junction. The design of the E/B heterojunction (HJ) can be classified into two categories: composition-graded,[3,4] and composition-abrupt junctions.[5,6] Ideally, the insertion of a composition-graded region at the E/B junction can eliminate the potential energy spike at the emitter side of the HJ, and thus increase the emitter injection efficiency. It has been shown both experimentally[7] and theoretically,[8] however, that the recombination current is also greatly enhanced in this case. From these previous results, the emitter injection efficiency is expected to decrease at low current, where the recombination current at the HJ is a limiting factor. Furthermore, the reduction of the potential spike also decreases the kinetic energy of the electrons injected from the emitter into the base.[9] This not only increases the transit time of electrons across the base (thereby limiting the device bandwidth), but also reduces the base transport factor.[6] The drop of both emitter injection efficiency and base transport factor is expected to limit the gain of the device, especially at low current levels.

As proposed by Kroemer,[9] the bulk recombination current at the E/B junction can be reduced by putting a high density of acceptor impurities at the heterointerface. In other words, if bulk recombination at the HJ is the major source of recombination current, we can improve the sensitivity and the speed of HPTs simply by growing composition-abrupt emitter layers with high-low carrier concentration profiles. The high-low emitter structure is similar in some respects to the double emitter, double base phototransistors proposed by Chen *et al.*[10] However, their structure was designed only to reduce the emitter/base capacitance without sacrificing the emitter injection efficiency, but the sensitivity of these HPTs is not expected to be improved beyond a conventional structure.[11] Furthermore, they fabricated this structure using GaAs/AlGaAs HPTs, where the surface recombination current in the extrinsic base region is believed to be the main source of recombination.[12] On the other hand, no dependence of the current gain on emitter perimeter-to-area ratio was observed for $In_{0.53}Ga_{0.47}As/InP$ bipolar transistors,[13] indicating that surface recombination current is negligible for this material system. Therefore, $InP/In_{0.53}Ga_{0.47}As$ HPTs are good candidates to demonstrate the effectiveness of structures which suppress bulk recombination.

In this letter, we describe both theoretical and experimental results of the effects on the photocurrent gain of inserting a thin, low-doped layer into the emitter of an $InP/In_{0.53}Ga_{0.47}As$ heterojunction phototransistor. The structure is called a high-low emitter (HILOE) HPT, and its cross section is shown in the inset of Fig. 1.

The simulation of the transistor operation is based on the drift-diffusion model,[14] where no tunneling through the potential barrier at the E/B junction is considered. The optical generation is assumed to be the only source of generation of electron hole pairs. Also, both SRH recombination and band-to-band recombination are included.

The collector current (I_c) of the HPT, when biased at voltage V_{CE} and illuminated by light incident with optical power P_i, can be calculated by solving the Poisson and continuity equations. The photocurrent gain (M), defined as the ratio of the number of photogenerated electrons to the number of incident photons, is calculated via

$$M = (I_c - I_D)h\nu/qP_i, \tag{1}$$

where I_D is the dark current, ν is the frequency of the incident photon, h is Planck's constant, and q is the electronic charge. It has been shown[15] that the photocurrent gain (M) is proportional to the collector current (I_c), viz. $M \propto I_c^{(1-1/n)}$. The slope of a plot of $\log(M)$ vs $\log(I_c)$,

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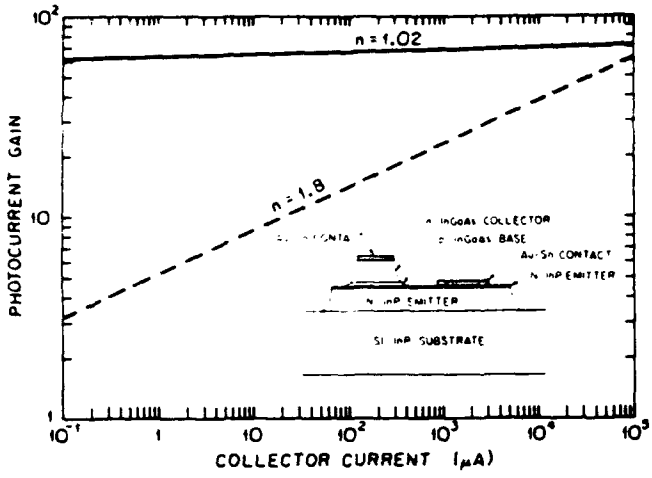

FIG. 1. Calculated comparison between HILOE (solid line) and conventional (dashed line) HPT gains vs collector current. (inset) Schematic cross-sectional view of HILOE-HPT.

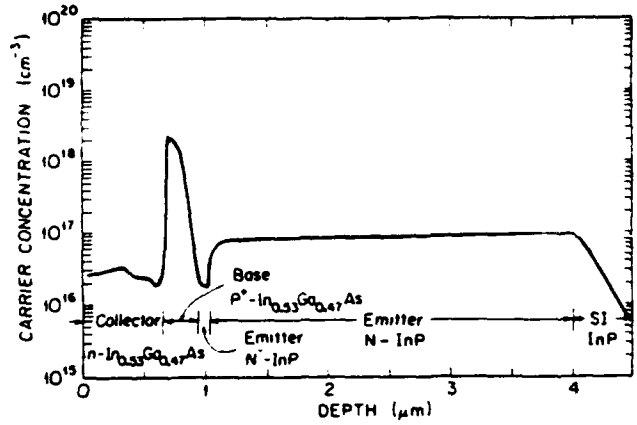

FIG. 2. Measured free-carrier concentration vs distance for the HILOE structure.

therefore, can give the ideality factor (n) of the HJ. For $n = 1$, bulk and surface recombination currents are small compared with the base diffusion current, whereas for $n \to 2$ the opposite situation is obtained.

For a conventional HPT, the doping concentrations of emitter, base, and collector used for simulation were assumed to be 4×10^{17} cm^{-3}, 1×10^{18} cm^{-3}, and 3×10^{16} cm^{-3}, and the layer thicknesses to be 2 , 0.2, and 2 μm, respectively. The HILOE-HPT consists of an additional N^--InP layer (of thickness d) inserted into the emitter of a conventional device. For this calculation, we take $d = 500$ Å and a doping concentration (N_{D2}) of 1×10^{16} cm^{-3} for the N^--InP layer. In Fig. 1, we present the values of M calculated for both the HILOE (solid line) and conventional (dashed line) HPTs using the approach discussed above. From the figure, we see that the gain of HILOE-HPT is only weakly dependent on the collector current, with $n = 1.02$ —an indication of diffusion current-dominated transport. On the other hand, the gain of the conventional HPT strongly depends on the collector current, with $n = 1.8$. This latter value of n is consistent with those typically observed for conventional InP/$In_{0.53}Ga_{0.47}As$ HPTs, either from our experimental results (see below), or those reported in the literature.[1] From this figure, we conclude that HILOE-HPT can reduce the recombination current and thus enhance the gain at low input optical power (and hence at low I_c).

The HILOE-HPT studied in this work (c.f., inset, Fig. 1) was grown on a (100) Fe-doped semi-insulating InP substrate by liquid phase epitaxy (LPE). In order to minimize the outdiffusion of the p dopant from the base into the low-doped emitter, Cd was used as the base dopant. The base doping concentration was 3×10^{18} cm^{-3}. Furthermore, the thin emitter layer is slightly Sn-doped to compensate the Cd out-diffused from the base. For wafer No. 1, a 2-μm-thick Sn-doped (2×10^{17} cm^{-3}) InP emitter was grown, followed by 0.1-μm-thick, Sn-doped (2×10^{16} cm^{-3}) N^--InP layer. Next, a 0.24-μm-thick, Cd-doped (2×10^{18} cm^{-3}) $In_{0.53}Ga_{0.47}As$ base, followed by a 0.7-μm-thick (2×10^{16} cm^{-3}) $In_{0.53}Ga_{0.47}As$ collector were grown. Wafer No. 2 was a conventional HPT structure with layer dopings and thicknesses similar to those of the HILOE device, with the exception of the thin extra emitter layer.

The doping concentration and layer thickness of each epitaxial layer was measured using an electrochemical profiler. Figure 2 shows the carrier concentration versus distance for wafer No. 1. The collector, base, and emitter regions are indicated in the figure. Note that a 0.1-μm-thick (2×10^{16} cm^{-3}) emitter layer region is clearly observed. This region is n type, implying that Sn indeed compensates the Cd diffused from the base. Furthermore, the built-in potential at the E/B junction was measured to be 0.93 eV. This value can be related to the conduction-band discontinuity energy (ΔE_c) via $\Delta E_c = qV_D - E_{g2} + \delta_1 + \delta_2$, where E_{g2} is the energy gap of $In_{0.53}Ga_{0.47}As$ and δ_1, δ_2 are the depths of the Fermi levels as measured from the conduction-band minimum for InP, and the valence-band maximum for $In_{0.53}Ga_{0.47}As$. From the calculation, ΔE_c is 0.22 eV, which is close to the value (0.24 eV) reported in the literature,[16] indicating that the E/B junction is abrupt. As has been pointed out,[17] the barrier height at the E/B junction is strongly affected by the p-type dopant diffusion into the emitter. Hence, the consistency of the measured ΔE_c with earlier data also implies that the use of Cd dopants can, indeed, reduce the displacement of the p/n junction away from the HJ.

After crystal growth and characterization of the epitaxial layers, a 50-μm-diam Au/Sn collector contact was deposited and patterned using metal lift-off. The collector mesa was defined by the collector contact, and citric acid was used to selectively etch both the n-$In_{0.53}Ga_{0.47}As$ and p-$In_{0.53}Ga_{0.47}As$ layers. The Au/Sn emitter contact was then formed on top of the emitter region, followed by isolating the emitter using a KKI solution ($HCL:CH_3COOH:H_2O_2$ in a ratio of 1:2:1). Finally, the metal contacts were alloyed at 425 °C for 1 min to reduce the contact resistance.

For the measurement of photocurrent gain, a 1.3 μm wavelength light-emitting diode (LED) was used as the light source, and optical powers of up to 2.5 μW were incident on the HPT via the substrate surface. The com-

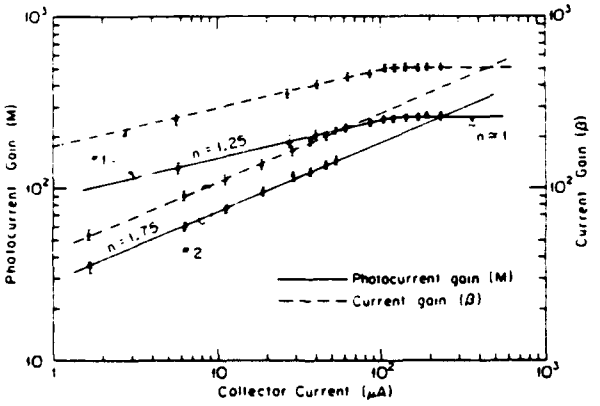

FIG. 3. Measured photocurrent gain (solid line) and current gain (dashed line) vs collector current (I_c) for both HILOE (wafer No. 1) and conventional (wafer No. 2) structures.

mon emitter characteristics of both wafers were measured and compared. A gain as high as 130 was obtained at an input power of only 40 nW for wafer No. 1. However, a gain of only 35 was measured at the same input optical power for wafer No. 2. In other words, an improvement of gain by a factor of 3.7 has been achieved at $P_i = 40$ nW using the HILOE structure.

Figure 3 shows M versus collector current (I_c) for both samples (solid lines). The photocurrent gain of wafer No. 1 is independent of I_c at high collector current, corresponding to $n = 1$. At low collector current, the gain was found to have a small current dependence, with $n = 1.25$. In contrast, the gain of wafer No. 2 decreases rapidly with collector current, and gives $n = 1.75$ over the entire range of I_c tested—a value typical of $InP/In_{0.53}Ga_{0.47}As$ HPTs grown by LPE[1] and consistent with the modeling results in Fig. 1. To our knowledge, the ideality factor of wafer No. 1 is the lowest value achieved for HPTs grown using LPE.

A conventional $In_{0.53}Ga_{0.47}As/InP$ HPT with $n = 1.2$ grown by gas source molecular beam epitaxy has also been reported.[13] This low n value is believed to be due to the high quality of the heterointerface obtained by this growth technique, which reduces the recombination current by increasing the minority-carrier lifetime at the interface. On the other hand, the HILOE structure we present here can reduce the recombination current simply by reducing the minority-carrier concentration at the HJ. In our case, the quality of heterointerface is not critical, thus reducing the dependence on the crystal growth technique employed.

For some devices on wafer Nos. 1 and 2, base contacts were formed. This enabled the measurement of quantum efficiency (η) by reverse biasing the base/collector junction and illuminating it with 1.3 μm wavelength light through the substrate side of the wafer. After the quantum efficiency measurement, the current gain (β), which is equal to M/η, was directly measured for both wafers. Results are shown in Fig. 3 (dashed lines). A high current gain of 260 was obtained at $P_i = 40$ nW for wafer No. 1, which is an improvement by a factor of 4.5 over the conventional device gain.

In conclusion, both theoretical and experimental results show that the growth of a thin, low-doped N^--InP layer in the emitter of a N-InP/P^--$In_{0.53}Ga_{0.47}As/n$-$In_{0.53}Ga_{0.47}As$ HPT can improve its optical sensitivity by diminishing the recombination current at the heterointerface. The significant gain enhancement of HILOE-HPTs indicates that both bulk and interface recombination currents at the emitter/base junction are the major sources of recombination for this material system.

The HILOE structure can also be applied to other material systems with high surface recombination currents (such as GaAs/AlGaAs) if a proper surface passivation technique is used. One of the strengths of the HILOE structure is that it can diminish the recombination current by reducing the minority-carrier concentration in the notch region of the HJ, rather than by increasing the minority-carrier lifetime. Hence, the performance of the HPT is less dependent on the quality of the heterointerface growth method used.

It has been pointed out[9] that the use of a graded base reduces the electron transit time which increases the bandwidth of the bipolar transistor. This idea has also been demonstrated successfully for the AlGaAs/GaAs HPT.[18] Hence the use of the double emitter layer with a high-low carrier concentration profile, along with a graded base will be expected to result in both a high sensitivity, and high bandwidth HPT.

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c. A high-gain, high-bandwidth $In_{0.53}Ga_{0.47}As/InP$ heterojunction phototransistor for optical communications

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We describe investigations of the effects of inserting a thin, low-doped layer into the emitter of an $InP/In_{0.53}Ga_{0.47}As$ heterojunction phototransistor (HPT). This high-low emitter structure has improved sensitivity and bandwidth over conventional structures at low input optical power by decreasing the bulk recombination current at the heterointerface. Experimental data show that the photocurrent gain is independent of the incident optical power at high input powers, corresponding to a heterojunction ideality factor of 1. At low input power, the gain is found to have a small power dependence, with an ideality factor of 1.25. A current gain as high as 260 is obtained at an input power of only 40 nW. These results, which are consistent with numerical simulations of the HPTs, give direct evidence that bulk recombination in the space- charge region at the emitter/base junction is the major source of recombination current for an $InP/In_{0.53}Ga_{0.47}As$ HPT A second structure is also proposed to improve the sensitivity by inserting a heavily doped layer into the base.

I. INTRODUCTION

Recently, there has been considerable interest in the development of heterojunction phototransistors (HPTs) as an alternative to *p-i-n* detectors for long-wavelength photoreceivers[1-4] since the HPT can provide large photocurrent gain[5] without the high bias voltages and excess avalanche noise characteristic of avalanche photodiode operation. Furthermore, the HPT is well suited to integration with heterojunction bipolar transistors in receivers or other circuits.

In optical fiber communications, the optical signal diminishes with distance, and the sensitivity of a photoreceiver drops at high frequency. In order to allow for large repeater separation and high-bandwidth operation, photoreceivers require high gain at low received optical powers; i.e., they require high sensitivity at low input optical power. It is well known,[1] however, that the photocurrent gain of a typical heterojunction phototransistor drops dramatically at low optical power, thereby limiting the sensitivity of the device. This behavior is attributed to different sources of recombination currents, such as Shockley–Read–Hall (SRH) recombination[6,7] through bulk defects, band-to-band radiative,[8] Auger,[9] and surface recombination currents[10,11] through surface states. The understanding of the relative contribution of each component to the total recombination current and the supression of major recombination sources, therefore, are the key to the improvement of the sensitivity of HPTs.

Under normal HPT operating conditions, the emitter/base (E/B) junction is forward biased, and most recombination occurs in the space-charge region (SCR) of this junction. The design of the E/B heterojunction (HJ) can be classified into two categories: composition-graded[12,13] and composition-abrupt junctions.[14,15] Ideally, the insertion of a composition-graded region at the E/B junction can eliminate the potential energy spike at the emitter side of the HJ and thus increase the emitter injection efficiency. It has been shown both experimentally[16] and theoretically,[17] however, that the recombination current is also greatly enhanced in this case. From these previous results, the emitter injection efficiency is expected to decrease at low current, where the recombination current at the HJ is a limiting factor. Furthermore, the reduction of the potential spike also decreases the kinetic energy of the electrons injected from the emitter into the base.[18] This not only increases the transit time of electrons across the base (thereby limiting the device bandwidth), but also reduces the base transport factor.[15] The drop of both emitter injection efficiency and base transport factor is expected to limit the gain of the device, especially at low-current levels.

As proposed by Kroemer,[18] the bulk recombination current at the E/B junction can be reduced by placing a high density of acceptor impurities at the heterointerface. In other words, if bulk recombination at the HJ is the major source of recombination current, we can improve the sensitivity and the speed of HPTs simply by either growing "composition-abrupt" double emitters forming an *N-P* homojunction or by growing emitter layers (or base layers) with high-low carrier-concentration profiles. The former structure has been demonstrated to improve the sensitivity of InGaAsP/InP HPTs,[3,19,20] and heterojunction ideality factors (n) as low as 1.49 have been obtained.[20] In this structure, the *p*-type impurities in the heavily doped base can diffuse into the emitter, thereby forming a thin *P*-InP emitter layer. However, this layer increases the effective base width (thereby reducing the base transport factor)

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and hence reduces the emitter injection efficiency.[19] Thus, the photocurrent gain may become small if the second emitter is too thick.[21] The need for critical thickness control of the second emitter rules out the practical use of this structure.

On the other hand, the high-low emitter (HILOE) structure is similar in some respects to the high-low emitter, low-high base phototransistors proposed by Chen *et al.*[22] Their structure was designed to reduce the emitter/base capacitance without sacrificing the emitter injection efficiency, but the sensitivity of these HPTs is not expected to show improvement over a conventional structure since the low-high base increases the recombination current at the HJ (see Appendix). Furthermore, they fabricated this structure using GaAs/AlGaAs HPTs, where the surface recombination current in the extrinsic base region is believed to be the main source of recombination.[23]

It has been shown that the surface recombination velocity of InP ($\sim 10^4$ cm/s) is two to three orders of magnitude smaller than that of GaAs ($\sim 10^6$ cm/s).[24] The minimum surface recombination velocity of $In_{0.53}Ga_{0.47}As$ is only 1–10 cm/s.[25] Furthermore, no dependence of the current gain on emitter perimeter–to–area-ratio has been observed for $In_{0.53}Ga_{0.47}As/InP$ bipolar transistors,[26] indicating that surface recombination current is negligible for this material system. Therefore, $InP/In_{0.53}Ga_{0.47}As$ HPTs are good candidates to demonstrate the effectiveness of structures which suppress bulk recombination.

In this paper, we fully describe both modeling calculations and experimental investigations of the effects on the photocurrent gain of an $InP/In_{0.53}Ga_{0.47}As$ heterojunction phototransistor modified by inserting a thin, low-doped layer into the HPT emitter. Preliminary results of this work have been reported earlier.[27]

This paper is organized as follows: In Sec. II, we present numerical simulation results comparing the photocurrent gain expected for the high-low doped emitter and conventional HPTs. The dependence of gain on layer thickness and doping concentration of the thin emitter are also studied. Furthermore, we show that the optimum choice of layer thickness and doping concentration can improve both photocurrent gain and gain-bandwidth product (f_T) of the HPT at low input optical power without degrading the frequency response at high input optical power. In Sec. III, the photocurrent gain of both HILOE and conventional HPTs at low input optical power are measured. We also discuss measurements on bipolar transistors with base contacts. These devices were used to measure the quantum efficiency of the HPTs and the current-voltage characteristics of the emitter/base junction. In Sec. IV, we present conclusions. Since the operation of the high-low base (HILOB) structure is similar to that of HILOE structure, simulation results concerning the former structure are presented in the Appendix.

II. DEVICE MODELING

The simulation of the transistor operation is based on the drift-diffusion model,[28–31] where no tunneling through the potential barrier at the E/B junction is considered. Also, both SRH recombination and band-to-band recombination processes are included. Recombination through deep levels follows the standard SRH formula.[6,7] The band-to-band recombination rate (U_{hb}), which includes radiative and Auger recombination, is given by

$$U_{hb}(x) = [B(x) - A_n(x)n - A_p(x)p](np - n_i^2), \quad (1)$$

where x is the distance from the emitter contact, B is the radiative recombination coefficient, and A_n and A_p are the Auger recombination coefficients for electrons and holes, respectively. Further, n and p are the position-dependent electron and hole densities, respectively, and n_i is the intrinsic carrier concentration. For simplicity, surface recombination in the extrinsic base region, which involves a two-dimensional calculation, is assumed to be zero. This is a good approximation for the $InP/In_{0.53}Ga_{0.47}As$ material system with its low surface recombination velocity.

The optical generation rate of electron-hole pairs [$G(x)$] is expressed by[32]

$$G(x) = \int_0^\infty T(\lambda)\phi(\lambda)\alpha(\lambda,x) \times \exp\left(-\int_0^\infty \alpha(\lambda,x')dx'\right)d\lambda, \quad (2)$$

where λ is the wavelength of the input light, $T(\lambda)$ is the optical transmission coefficient of the InP emitter layer, $\phi(\lambda)$ is the incident light flux, and $\alpha(\lambda,x)$ is the absorption coefficient of the $In_{0.53}Ga_{0.47}As$ base and collector layers.

The collector current (I_c) of the HPT, when biased at voltage V_{CE} and illuminated by light incident with optical power P_i, can be calculated by solving the Poisson and continuity equations.[33] The photocurrent gain (M), defined as the ratio of the number of collected electrons to the number of incident photons, is calculated via

$$M = (I_c - I_D)h\nu/qP_i, \quad (3)$$

where I_D is the dark current, ν is the frequency of the incident photon, h is Planck's constant, and q is the electronic charge.

The material parameters used in the following calculation for InP and $In_{0.53}Ga_{0.47}As$ are listed in Table I. According to our simulation, the electron diffusion length (L_n) in the base region, which determines the electron lifetime and, in turn, the base recombination current, is the most critical parameter for calculating the photocurrents. In the literature, the measured values of L_n in the p-$In_{0.53}Ga_{0.47}As$ layer ($\sim 2\ \mu$m) are in good agreement[35,38] at a doping concentration of 1×10^{18} cm^{-3}, and thus we use this value for simulation. Moreover, the calculated heterojunction ideality factor of the conventional HPTs (see below) is consistent with our experimental data, which further support the assumption that $L_n = 2\ \mu$m in the base layer is a reasonable value.

On the other hand, the measured hole diffusion length (L_p) and hole lifetime (τ_p) in N-InP show a large variation in the literature,[39] where L_p ranges from $< 1\ \mu$m to $> 20\ \mu$m in the doping concentration range of from 1×10^{16} to 5×10^{17} cm^{-3}. The considerable discrepancy in these data

TABLE I. Parameters used for transistor simulation.

Parameter	Symbol	InP	$In_{0.53}Ga_{0.47}As$
Energy gap	E_g (eV)	1.35	0.75
Electron effective mass ratio	m_n^*/m_0	0.08	0.041
Hole effective mass ratio[a]	m_p^*/m_0	0.56	0.50
Dielectric constant	ϵ_r/ϵ_0	12.3	12.0
Electron mobility[a]	μ_n ($cm^2/V\,s$)		
$N_D + N_A = 10^{16}$		4100	10 500
10^{17}		3500	9000
10^{18}		2400	5000
Hole mobility[a]	μ_p ($cm^2/V\,s$)		
$N_D + N_A = 10^{17}$		150	300
10^{18}		80	130
Electron diffusion length in p-$In_{0.53}Ga_{0.47}As$[b] $N_D + N_A = 10^{18}$	L_n (μm)	...	2
Hole diffusion length in n-InP[b] $N_D + N_A = 10^{16}$–10^{17}	L_p (μm)	2.4	...
Radiative recombination coefficient[c]	B (cm^3/s)	1.65×10^{-11}	4.2×10^{-11}
Auger recombination coefficient[d] (n type)	A (cm^6/s)	4×10^{-30}	1.67×10^{-27}
Auger recombination coefficient[d] (p type)	A (cm^6/s)	2.4×10^{-30}	1×10^{-27}
Absorption coefficient at 1.3 μm wavelength[e]	α (cm^{-1})	0	1.5×10^4

[a] See Ref. 34.
[b] See Ref. 35.
[c] See Ref. 36 for 1.3-μm InGaAsP. The radiative lifetime is proportional to the square of wavelength, and thus the radiative coefficient for both $In_{0.53}Ga_{0.47}As$ and InP can be obtained.
[d] See Ref. 9.
[e] See Ref. 37.

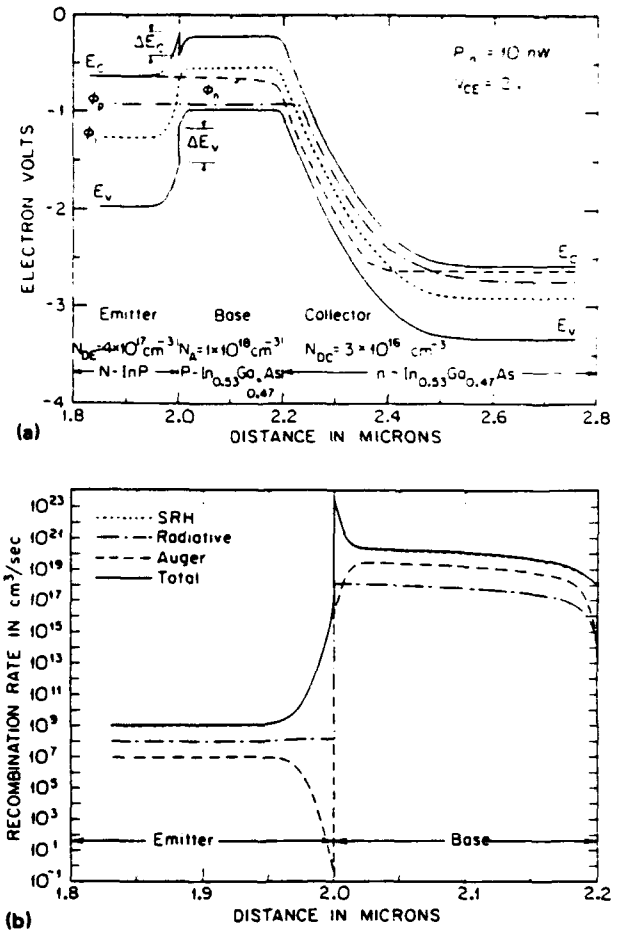

FIG. 1. Calculated (a) energy-band diagram and (b) recombination rate near the heterojunction of a typical N-InP/p^+-$In_{0.53}Ga_{0.47}As$/n-$In_{0.53}Ga_{0.47}As$ HPT, biased at $V_{CE} = 2$ V and illuminated by $P_i = 10$ nW, 1.3-μm- wavelength light. The intrinsic quasi-Fermi level (ϕ_i), and the electron (hole) quasi-Fermi level ϕ_n (ϕ_p), are also indicated in (a).

has been attributed to different material quality and measurement techniques.[39] However, our simulation results indicate that they are very insensitive to the value of L_p (and thus τ_p), consistent with the fact that the contribution of emitter recombination current to the total current is negligible (see below). For example, as L_p changes from 2.4 to 0.24 μm, the difference in the photocurrents for both cases is less than 1%, even at the input optical power of 0.01 μW, where the recombination current is dominant. Here, we use $L_p = 2.4$ μm (Ref. 35) in the N-InP layer in the doping concentration range of 1×10^{16}– 1×10^{17} cm^{-3}.

Figure 1(a) shows the calculated energy-band diagram of a typical N-InP/p^+-$In_{0.53}Ga_{0.47}As$/n-$In_{0.53}Ga_{0.47}As$ HPT, biased at $V_{CE} = 2$ V and illuminated by 1.3-μm wavelength light at $P_i = 10$ nW. The intrinsic quasi-Fermi level (ϕ_i), and the electron (hole) quasi-Fermi level, ϕ_n (ϕ_p) are also indicated. Here, the doping concentrations of emitter, base, and collector are 4×10^{17}, 1×10^{18}, and 3×10^{16} cm^{-3}; and the layer thicknesses are 2, 0.2, and 2 μm, respectively. As shown in the figure, a "spike" and "notch" conduction-band energy profile is apparent at the InP/$In_{0.53}Ga_{0.47}As$ HJ, where a conduction-band discontinuity energy (ΔE_c) of 0.24 eV (Ref. 40) was used. Under normal operating conditions, light is incident via the wide-band gap, transparent emitter, and is then absorbed in the base and collector regions, creating electron-hole pairs. The presence of the large barrier (1.3 eV) in the valence band results in the accumulation of photogenerated holes, thereby allowing electrons to be injected from the emitter. At very low input powers, bulk recombination limits the

emitter injection efficiency, and a photocurrent gain of only 5.1 is calculated for this device.

Figure 1(b) shows the recombination rate near the HJ calculated using the energy-band diagram of Fig. 1(a). Each component of the recombination rate, as well as the total recombination rate, is indicated. Note that the SRH recombination rate is much higher than the radiative and Auger recombination rates throughout the device. Furthermore, the total recombination rate ($\sim U_{SRH}$) increases dramatically in the notch region. This can be explained by recalling that, at low minority-carrier injection, U_{SRH} can be simply expressed as $(p - p_{n0})/\tau_p$ in the emitter, and $(n - n_{p0})/\tau_n$ in the base,[33] where p_{n0} and n_{p0} are the equilibrium minority-carrier concentrations in the emitter and base, respectively. Also, τ_n (τ_p) is the electron (hole) carrier lifetime. Hole injection from the base into the emitter is limited by the large barrier in the valence band, and thus the recombination rate is negligible in both the space-charge and neutral emitter regions. On the other hand, the electrons injected from the emitter are trapped in the notch, thereby increasing the recombination rate dramatically. As electrons pass through the quasineutral base, the recombination of electrons and holes reduces the electron concentration, and as shown in the figure, the recombination rate decreases. Also note that the Auger recombination rate is smaller than the radiative recombination rate in the emitter, although it is larger in the base where a high density of p-type dopants is present.

The above analysis assumes that the minority-carrier lifetime is independent of position for both materials. However, the existence of interface states at the HJ can reduce the minority-carrier lifetime at the interface and can thus cause more recombination than that calculated above. Therefore, the elimination of the notch at the base side of the HJ is essential for reducing the total recombination current.

Figure 2(a) illustrates the energy-band diagram of the HILOE HPT consisting of an additional N^--InP layer (of thickness, d) inserted into the emitter of a conventional device. For this calculation, we take $d = 500$ Å and a doping concentration (N_{D2}) of 1×10^{16} cm^{-3} for the N^--InP layer. As before, $V_{CE} = 2$ V and $P_i = 10$ nW are assumed. This low-doped layer has the effect of repelling electrons from both sides of the E/B junction. Comparison of Figs. 1(a) and 2(a) indicates that the SCR is wider on the emitter side of the HJ, and more importantly, the notch depth is reduced in the HILOE structure. Note that the spike in the conduction-band energy profile at the emitter side of the HJ is above the potential energy in the base region. The current transport across the HJ is thus hindered by this larger barrier, and the electron quasi-Fermi level (ϕ_n) shows a steplike drop at the interface. However, this does not imply that fewer electrons are injected from the emitter. On the contrary, a photocurrent gain of 64 was calculated in this case—an enhancement of gain over the conventional HPT by more than a factor of 10. This is explained using Fig. 2(b), showing the recombination rate near the HJ. Again, SRH recombination is the main source of recombination. However, the peak value of the recombination rate at the HJ has dropped from 1×10^{24} to 2×10^{22} cm^3/s by the insertion of the thin emitter layer.

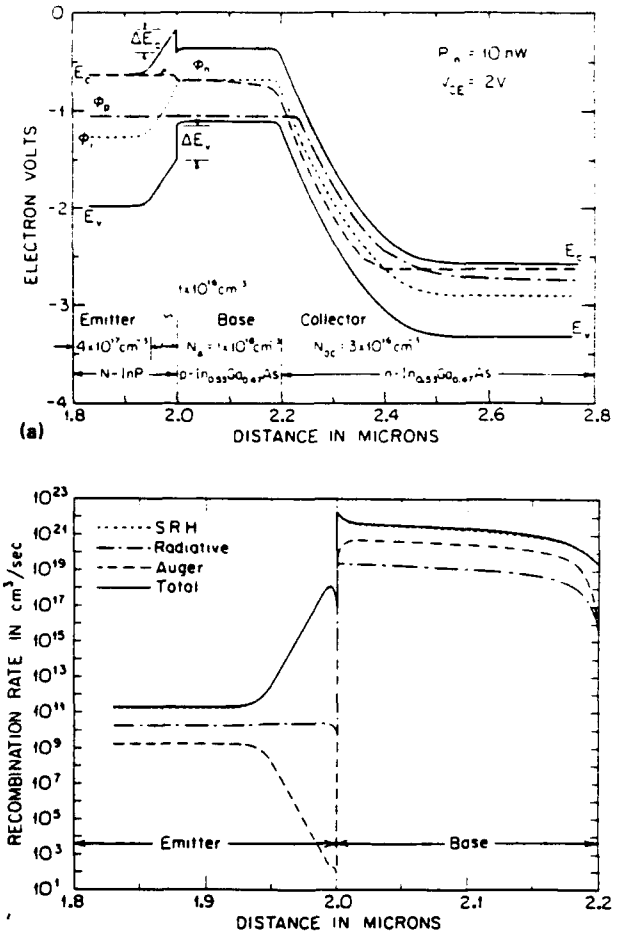

FIG. 2. Calculated (a) energy-band diagram and (b) recombination rate near the heterojunction of the HILOE HPT consisting of an additional N^--InP layer inserted into the emitter of a conventional device. For this calculation, we take an N^--InP layer thickness (d) of 500 Å and a doping concentration (N_{D2}) of 1×10^{16} cm^{-3}. As in Fig. 1, $V_{CE} = 2$ V and $P_i = 10$ nW are assumed.

Figure 3 shows the calculated common emitter characteristics of the HILOE-HPT, using the same parameters as those used in Figs. 1(b) and 2(b). The input optical power is labeled for each curve. As shown in the figure, the gain (M) is nearly independent of input power, as desired for high sensitivity.

In general, the current (I) of a forward-biased E/B junction can be expressed as

$$I = A_1 \exp(qV_{BE}/n_1 k_B T) + A_2 \exp(qV_{BE}/n_2 k_B T), \quad (4)$$

where $n_1 \simeq 1$, $n_2 \simeq 2$, V_{BE} is the voltage drop at E/B junction, and A_1 and A_2 are the prefactors of both current components. The first term of Eq. (4) is due to diffusion current across the junction, and the second term originates from the recombination current. Equation (4) implies that I is approximately proportional to $\exp(qV_{BE}/nk_BT)$, where n is the ideality factor of the HJ. For $n = 1$, bulk and

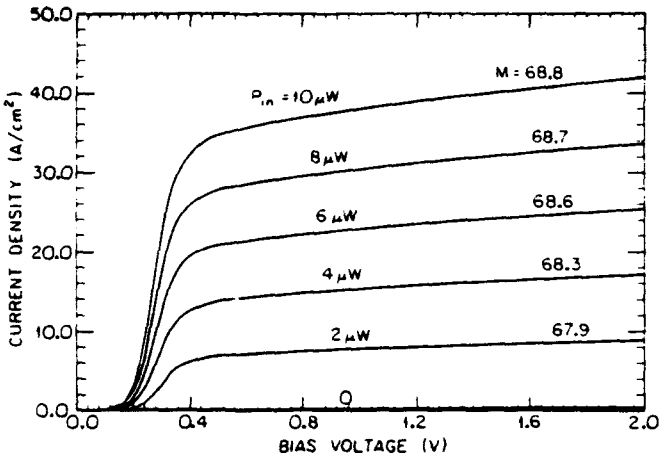

FIG. 3. Calculated common emitter characteristics of the HILOE HPT, using the same parameters as those used in Figs. 1(b) and 2(b).

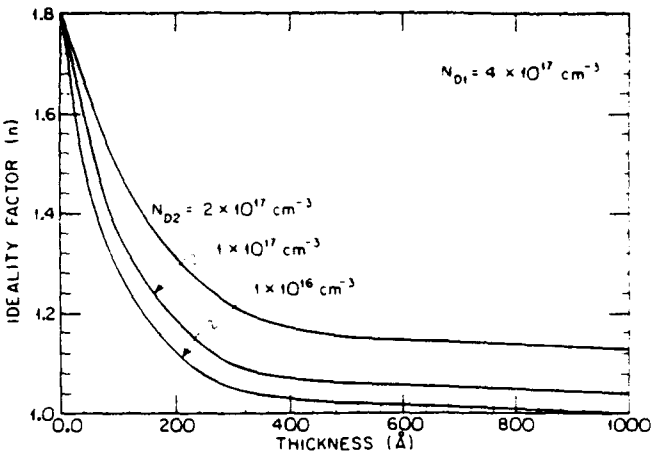

FIG. 5. Calculated heterojunction ideality factors (n) for different layer thicknesses (d) and doping concentrations (N_{D2}) of the low-doped emitter layer.

surface recombination currents are small compared with the base diffusion current, whereas for $n \to 2$ the opposite situation applies.

Furthermore, it can be shown[41] that the photocurrent gain (M) is proportional to the collector current (I_c), viz., $M \propto I_c^{(1-1/n)}$. The slope of a plot of $\log(M)$ vs $\log(I_c)$, therefore, can give the ideality factor (n) of the HJ. In Fig. 4, M is calculated for both HILOE and conventional HPTs using the approach discussed above. The gain of the HILOE HPT is only weakly dependent on the collector current with $n = 1.02$—an indication of diffusion current-dominated transport. On the other hand, the gain of the conventional HPT strongly depends on the collector current, with $n = 1.8$. This latter value is consistent with those typically observed for conventional $InP/In_{0.53}Ga_{0.47}As$ HPTs, either from our experimental results (see below) or from those reported in the literature.[1] From this figure and the previous analysis, we conclude that the HILOE structure can significantly reduce the recombination current and thus enhance the gain at low input optical powers (i.e., low I_c).

Note that the difference in M between the conventional and HILOE HPTs decreases at high collector currents (or high input optical powers), as indicated in the same figure. In this high-current region, the recombination current is negligible compared with the diffusion current. Here, electrons injected from the emitter are hindered by the large potential spike at the E/B junction. However, increasing the sensitivity of HPTs at low optical input power is of greater importance to the utility of the device in optical communication applications.

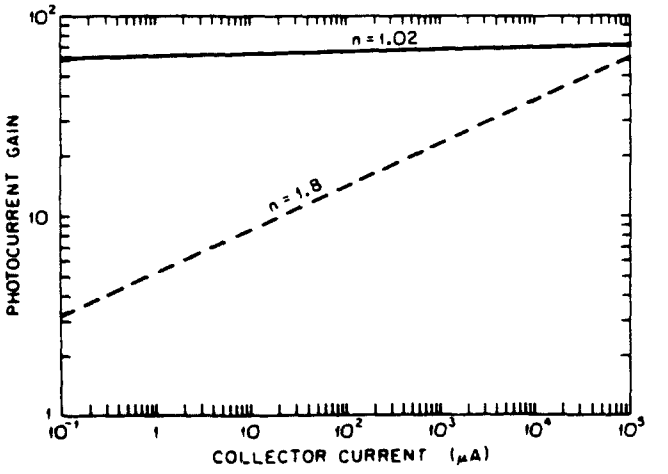

FIG. 4. Calculated comparison between HILOE (solid line) and conventional (dashed line) HPT gains, using the same parameters as those used in Figs. 2(a) and 1(a), respectively.

The effect of layer thickness (d) and doping concentration (N_{D2}) of the low-doped emitter layer on n is shown in Fig. 5. Here, n approaches unity by increasing the layer thickness (d) or decreasing the doping concentration (N_{D2}) of the thin emitter layer. If N_{D2} is low, n drops rapidly with increasing layer thickness. For example, $n = 1.05$ can easily be achieved simply by growing a 300-Å-thick layer with $N_{D2} = 1 \times 10^{16}$ cm^{-3} into the emitter.

According to this figure, the recombination current can be efficiently reduced by growing a thick undoped emitter layer into the emitter. In this case, however, the depletion edge at the emitter side ends within the undoped emitter, thereby increasing the emitter series resistance, which in turn degrades the frequency response of the HPT. Hence, the optimum design of layer thickness and doping concentration of the thin emitter layer is essential to obtain a combination of high sensitivity and bandwidth.

The gain-bandwidth product (or cutoff frequency) f_T, defined as the frequency at which the current gain is unity, is one figure of merit used to describe the high-frequency performance of the bipolar transistor. Here, f_T depends on the total emitter-to-collector transit time and can be calculated via[42]

$$f_T = 1/2\pi[(R_{EC} + R_{EB})C_c + r_{ed}(C_E + C_c) + W_B^2/2D_n + (R_{cc} + R_{cB})C_c + W_{BC}/2v_s]^{-1}, \quad (5)$$

where R_{EC}, R_{EB}, and r_{ed} are the contact, bulk, and dynamic resistances of the emitter layer; R_{cc} and R_{cB} are the contact and bulk resistances of the collector; C_E and C_c are the

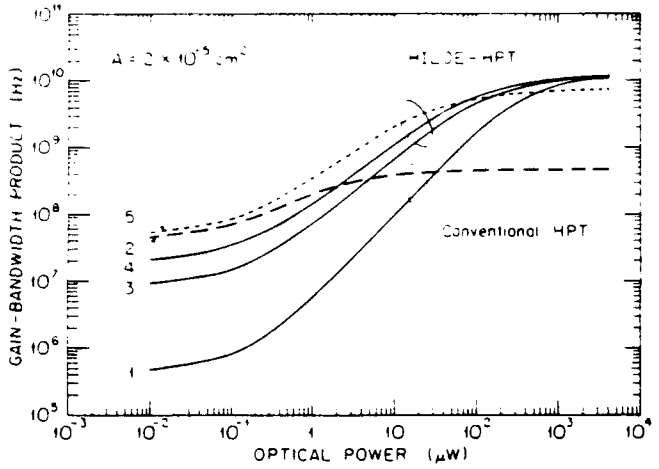

FIG. 6. Calculated gain-bandwidth products (f_T) at different input optical powers (P_i) for both conventional and HILOE HPTs. Curves 1 and 2 represent the conventional HPT with $N_D = 4 \times 10^{17}$ and 1×10^{16} cm^{-3}, respectively. Curves 3, 4, and 5 are for HILOE HPTs with $N_{D2} = 2 \times 10^{17}$ cm^{-3}, $d = 0.1$ μm, $N_{D2} = 1 \times 10^{17}$ cm^{-3}, $d = 0.1$ μm, and $N_{D2} = 1 \times 10^{16}$ cm^{-3}, $d = 1$ μm, respectively.

capacitances of the emitter-base and base-collector junctions, W_B is the base width, W_{BC} is the depletion width of the base/collector junction, D_n is the diffusion coefficient of electrons in the collector region, and v_s is the saturation velocity of electrons in the collector region. The first and the second terms of Eq. (5) correspond to the emitter charging time (τ_E), and other terms correspond to the base transit (τ_B), collector charging (τ_C), and collector depletion layer transit times (τ_{SCR}).

For a floating base HPT, the emitter current (I_E) is equal to collector current (I_c). Thus, the dynamic emitter resistance ($r_{ed} = nk_BT/qI_E$) can be approximated by $nhvk_BT/q^2MP_i$, where Eq. (3) is used for calculating I_c. At low input optical power (P_i), the dynamic emitter resistance (r_{ed}) is large, and the response time is limited by the emitter charging time, thereby degrading the frequency response of the HPT. In this case, the second term in Eq. (5) dominates, and f_T is proportional to the photocurrent gain-power product (MP_i). On the other hand, the dynamic resistance is negligible at high input optical power, and f_T becomes constant with $f_T = f_T(\max)$. This power dependence of f_T has been reported both experimentally[43] and theoretically.[44] However, the calculation of f_T in Ref. 44 assumes that the emitter injection efficiency is unity. In the following, we take the recombination current at the HJ into account for calculating M and, in turn, f_T.

In Fig. 6, f_T is calculated for different input optical powers (P_i) for both conventional and HILOE HPTs. The HILOE-HPT used for simulation is based on the structure we fabricated (cf. inset of Fig. 7), where the junction areas of both collector/base and emitter/base are 2×10^{-5} cm^2, and the separation of the emitter to the collector contact is 25 μm. The doping concentrations and layer thicknesses of each layer are the same as those used in Fig. 1, and the junction capacitances C_E and C_c are calculated at $V_{CE} = 1.6$ V. The sheet resistance of the high-low doped emitter layer was calculated, and in turn, R_{EB} was obtained.

As shown in the figure, the gain-bandwidth product of the conventional HPT with an emitter doping concentration of $N_D = 4 \times 10^{17}$ cm^{-3} (curve 1) is less than 1 MHz at $P_i = 10$ nW. As P_i increases, f_T slowly increases in the low-input-power region, where the photocurrent gain is limited by the bulk recombination current at the HJ ($n = 1.8$), and increases more rapidly at high input powers. Finally, f_T saturates at $P_i > 1$ mW, where $f_T = f_T(\max) = 11$ GHz in this case. The response of a second conventional HPT with $N_D = 1 \times 10^{16}$ cm^{-3} (curve 2) is also shown in the same figure for comparison. In this case, the enhanced photocurrent gain at low input power ($n = 1.01$) and the lower value of C_E improve the gain-bandwidth product. On the other hand, the large emitter series resistance (R_{EB}) of this low-doped emitter layer limits the emitter charging time and, thus, $f_T = 0.44$ GHz at high input optical power.

The gain-bandwidth product of three HILOE HPTs with $N_{D2} = 2 \times 10^{17}$ cm^{-3}, $d = 0.1$ μm (curve 3), $= 1 \times 10^{17}$ cm^{-3}, $d = 0.1$ μm (curve 4), and $N_{D2} = 1 \times 10^{16}$ cm^{-3}, $d = 1$ μm (curve 5) are also shown in the same figure. The ideality factor (n) of each curve corresponds to 1.13, 1.04, and 1.02, respectively. Note that by either increasing the layer thickness or decreasing the doping concentration of the low-doped emitter layer, the photocurrent gain, and thus the gain-bandwidth product, is greatly improved at low input optical power. For curves 3 and 4, the emitter series resistance is small and the maximum gain-bandwidth product at high input power is 11 GHz for both cases. On the other hand, the degradation in $f_T(\max)$ is clearly observed for the device with $N_{D2} = 1 \times 10^{16}$ cm^{-3} (curve 5).

Ideally, the gain-bandwidth product of the conventional HPT can be improved by supplying the base current to reduce the dynamic emitter resistance. This can be achieved with an external dc light source (optically),[45] or by adding a base contact (electrically).[46] However, both techniques dissipate more power and increase HPT shot noise. The base contact of the latter technique also increases the junction area (and hence capacitance), as well as the lateral series resistance, both of which degrade the frequency performance. On the other hand, the HILOE HPT avoids both of these problems.

From Figs. 5 and 6, we conclude that the layer thickness (d) and doping concentration (N_{D2}) of the low-doped emitter can be optimized to improve both sensitivity and gain-bandwidth product at low input optical power without degrading the frequency response of the HPT at high input optical power.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Heterojunction phototransistor performance

The phototransistor studied in this work (inset, Fig. 7) was grown on a (100) Fe-doped semi-insulating InP substrate by liquid-phase epitaxy (LPE). In order to minimize the out-diffusion of the p dopant from the base into the

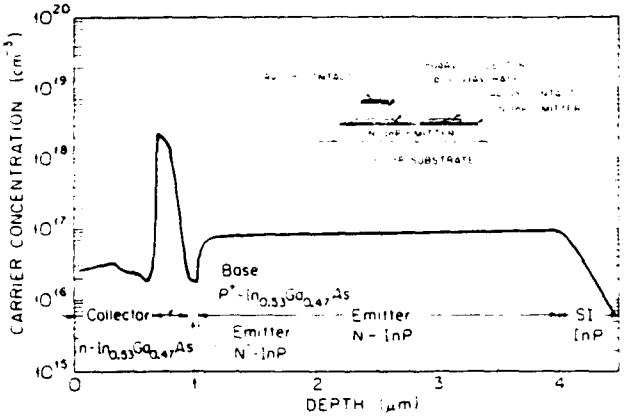

FIG. 7. Measured free-carrier concentration vs distance for the novel structure. Inset: Schematic cross sectional view of the HILOE HPT.

low-doped emitter, Cd was used as the base dopant. The base doping concentration was 3×10^{18} cm^{-3}. Furthermore, the thin emitter layer is slightly Sn doped to compensate the p dopants which unavoidably diffuse from the base. For wafer No. 1, a 2-μm-thick Sn-doped (2×10^{17} cm^{-3}) InP emitter was grown, followed by 0.1-μm-thick, Sn-doped (2×10^{16} cm^{-3}) N^--InP layer. Next, a 0.24-μm- thick, Cd-doped (2×10^{18} cm^{-3}) $In_{0.53}Ga_{0.47}As$ base, followed by a 0.7-μm-thick (2×10^{16} cm^{-3}) $In_{0.53}Ga_{0.47}As$ collector were grown. Wafer No. 2 was a conventional HPT structure with layer dopings and thicknesses similar to those of wafer No. 1 except that the thin extra emitter layer is omitted in wafer No. 2.

The doping concentration and layer thickness of each epitaxial layer was measured using an electrochemical profiler. Figure 7 shows the carrier concentration versus distance for wafer No. 1. The collector, base, and emitter regions are indicated in the figure. Note that a 0.1-μm-thick (2×10^{16} cm^{-3}) layer is clearly observed at the E/B junction. This InP region is n type, implying that Sn indeed compensates the Cd diffused from the base. Furthermore, the built-in potential at E/B junction was measured to be 0.93 eV. This value can be related to the conduction-band discontinuity energy (ΔE_c) via $\Delta E_c = qV_D - E_{g2} + \delta_1 + \delta_2$,[47] where E_{g2} is the energy gap of $In_{0.53}Ga_{0.47}As$, and δ_1 and δ_2 are the depths of the Fermi levels as measured from the conduction-band minimum for InP and the valence-band maximum for $In_{0.53}Ga_{0.47}As$, respectively. Here, δ_1 and δ_2 can be calculated using an approximation to the Fermi–Dirac distribution, from which $\delta_1 = 2\times10^{-3}$ eV and $\delta_2 = 0.04$ eV are obtained. Using this analysis, ΔE_c is found to be 0.22 eV, which is close to the value (0.24 eV) reported in the literature,[40] indicating that the E/B junction is abrupt. As has been pointed out earlier,[48] the barrier height at the E/B junction is strongly affected by the p-type dopant diffusion into the emitter. Hence, the consistency of the measured ΔE_c with earlier data gives further support to the observation that Cd dopants can, indeed, reduce the displacement of the p/n junction away from the HJ.[21,49]

The electrochemical profiling technique was also applied to wafer No. 2, and in contrast, the carrier-concentration profile does not show any dip at the E/B junction (cf. Fig. 7). For comparison, the thickness and doping concentration of each epitaxial layer for both wafers are listed in Table II.

TABLE II. Summary of parameters for wafers No. 1 and No. 2.

Region	Material	Layer thickness[a] (μm) Wafer No. 1	Layer thickness[a] (μm) Wafer No. 2	Doping concentration ($\times10^{18}$ cm^{-3}) Wafer No. 1	Doping concentration ($\times10^{18}$ cm^{-3}) Wafer No. 2
Collector	n-InGaAs (Sn doped)	0.67	1.9	2.3	2
Base	p-InGaAs (Cd doped)	0.24	0.20	200	300
Emitter	N-InP (Sn doped)	2.8	3.0	10	10

[a]The thickness of each epitaxial layer was measured by both electrochemical and step profiler methods. They showed good agreement.

After characterization of the epitaxial layers, a 50-μm-diam Au/Sn collector contact was deposited and patterned using metal lift-off. The transistor mesa was defined by the collector contact, and citric acid was used to selectively etch both the n-$In_{0.53}Ga_{0.47}As$ and p-$In_{0.53}Ga_{0.47}As$ layers. An Au/Sn emitter contact was then formed on top of the emitter region, followed by isolating the emitter using KKI solution ($HCL:CH_3COOH:H_2O_2$ in a ratio of 1:2:1). Finally, the metal contacts were alloyed at 425 °C for 1 min to reduce the contact resistance.

For the measurement of photocurrent gain, a 1.3-μm-wavelength LED was used to illuminate the HPT via the substrate surface. The common emitter characteristics of wafer No. 1 are shown in Fig. 8. In the figure, the photocurrent gain drops from 255 to 130 as the input optical power (P_i) decreases from 0.54 to 0.04 μW. These results are in contrast to a gain of only 35 measured at 0.04 μW for wafer No. 2 which is close to the best result ($M = 40$ at $P_i = 40$ nW) for the conventional HPTs reported to date.[21]

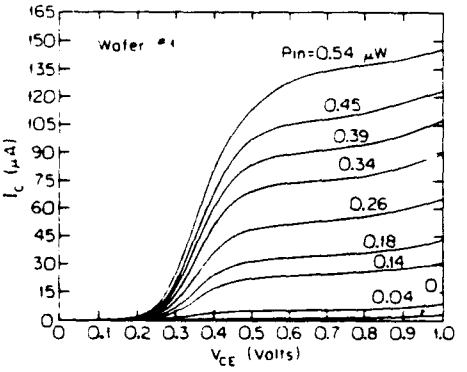

FIG. 8. Typical common emitter characteristics for wafer No. 1 (HILOE HPT).

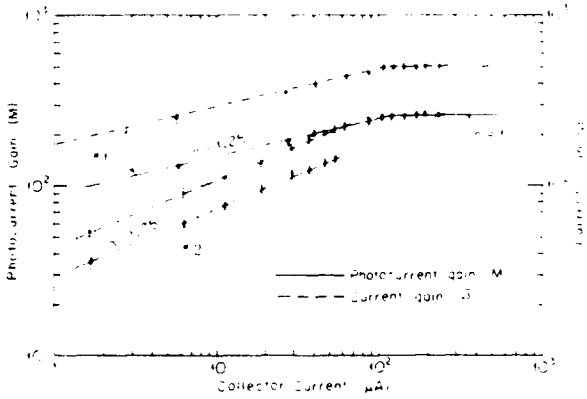

FIG. 9. Measured photocurrent gain (solid line) and current gain (dashed line) vs collector current (I_c) for both HILOE (wafer No. 1) and conventional (wafer No. 2) structures.

In other words, an improvement of gain by a factor of 3.7 has been achieved at $P_i = 40$ nW using the HILOE structure.

Figure 9 shows M versus collector current (I_c) for both samples (solid lines). As expected, the photocurrent gain of wafer No. 1 is independent of I_c at high collector current, corresponding to $n = 1$. At low collector current, the gain was found to have a small current dependence, with $n = 1.25$. In contrast, the gain of wafer No. 2 decreases rapidly with collector current and gives $n = 1.75$ over the entire range of I_c tested—a value typical of InP/$In_{0.53}Ga_{0.47}As$ HPTs grown by LPE,[1] and consistent with the modeling results in Fig. 4. To our knowledge, the ideality factor of wafer No. 1 is the lowest value achieved for HPTs grown using LPE.

Campbell, Tsang, and Qua, fabricated an InP/$In_{0.53}Ga_{0.47}As$ HPT grown by chemical beam epitaxy (CBE) with $n = 1.14$.[50] However, for that device the emitter layer was undoped, which accounts for the low n value. Further, the large series emitter resistance is also expected to lead to reduced bandwidth response (cf. curves 1 and 2 in Fig. 6). In other work, a conventional $In_{0.53}Ga_{0.47}As$/InP HPT with $n = 1.2$ was grown by gas-source molecular-beam epitaxy (MBE). Here, the emitter carrier concentration was 2×10^{17} cm^{-3}. In this case, the low n value is believed to be due to the high quality of the heterointerface obtained by this growth technique, which reduces the recombination current by increasing the minority-carrier lifetime at the interface. On the other hand, the transistor structure in Fig. 7 can reduce the recombination current simply by reducing the minority-carrier concentration at the HJ. Here, the quality of heterointerface is not critical, thus reducing the dependence on the crystal growth technique employed.

In order to study the properties of the base/collector homojunction and the emitter/base heterojunction, base contacts were formed for devices on both wafers No. 1 and No. 2. This enabled the measurement of quantum efficiency (η) by reverse biasing the base/collector junction and illuminating the junction with 1.3-μm-wavelength light through the substrate side of the wafer. From the quantum efficiency, the current gain (β), which is equal to M/η,[51] was calculated. A high-current gain of 260 was obtained at $P_i = 40$ nW for wafer No. 1 (Fig. 9), which is an improvement by a factor of 4.5 over the conventional device gain. To our knowledge, the current gain of wafer No. 1 is the highest value reported in the literature for this low level of optical power.

B. Current-voltage characteristics of the emitter/base junction

We can independently determine n and the sources of recombination in these structures by studying the forward-biased (dark) I-V characteristics of the E/B junction. Thus, in Figs. 10(a) and 10(b), we compare the forward I-V characteristics of the emitter/base junctions for both wafers. For wafer No. 1, $n = 2.5$ at $V_{BE} \leqslant 0.2$ V (region I), as shown in Fig. 10(a). The large value of n indicates that base recombination current [the second term of Eq. (4)] in this low-current region is dominant. At these low voltages, the bias voltage is less than the offset voltage of the HPT (cf. Fig. 8), and hence this region was not accessible to the measurements used to obtain the data in Fig. 9.

In region II, where the bias voltage is between 0.2 and 0.4 V, $n = 1.3$, which is consistent with $n = 1.25$ in the low-I_c collector current region of wafer No. 1, shown in Fig. 9. If the recombination current in this region originates from the same sources as in region I, we can extract it from the total current simply by extrapolating the current level of region I into region II [dashed line in Fig. 10(a)]. After subtracting the recombination current from the total current, the ideality factor ($n = 1.05$) of the new curve is very close to 1, corresponding to the diffusion current [cf. Eq. (4)]. In the figure, we clearly see that diffusion current dominates the recombination current in region II.

At high forward voltages, the resistance of the low-doped emitter and the lateral base resistance limit the diffusion current, causing the current to saturate in region III. For the HPT of wafer No. 1, current flows through the base region vertically, not laterally. This leads to less series resistance, and thus the ideality factor of $n = 1$ can be observed even at high collector currents.

In contrast, the ideality factor of wafer No. 2 is $n = 2.6$ in region I ($V_{BE} \leqslant 0.35$ V), as shown in Fig. 10(b). Although the ideality factor is the same as that of wafer No. 1 in region I, the recombination current is 250 times larger, and the voltage range where the recombination current dominates is also larger. In region II, $n = 2.1$, corresponding to the low-collector-current region of wafer No. 2 in Fig. 9. After subtracting the recombination current from the total current, we once more obtain $n = 1.05$, due to the diffusion current. By comparing the diffusion currents of both wafers, note that wafer No. 2 has a higher current than that of wafer No. 1. This results since the voltage drop in the low-doped emitter region for wafer No. 1 reduces V_{BE} and, in turn, the diffusion current.

From the above analysis, the recombination current at the HJ has been reduced by *two orders of magnitude* for the

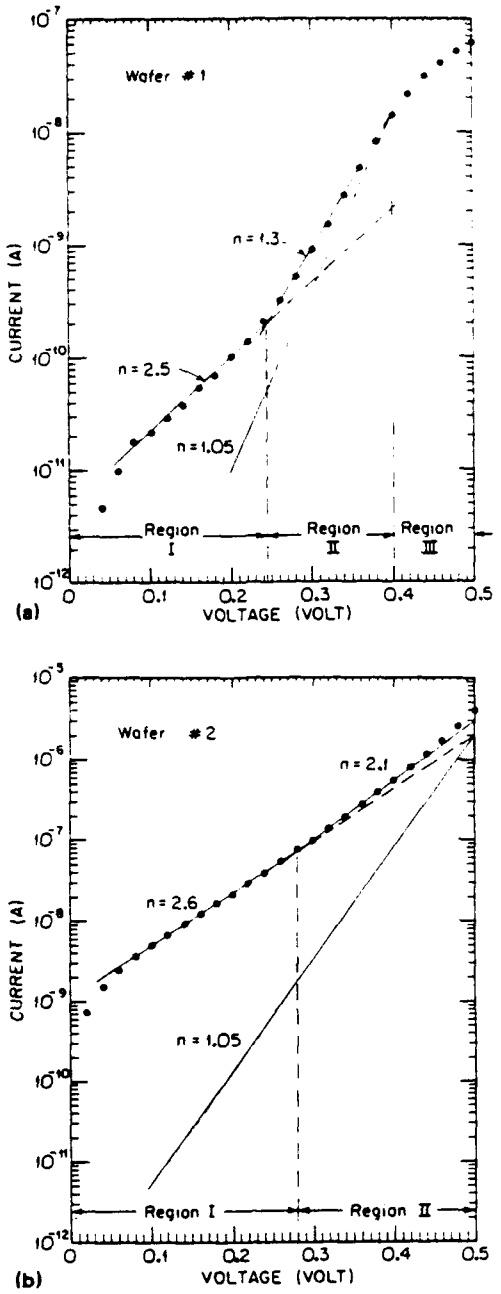

FIG. 10. Forward-biased I-V characteristics of the emitter/base junction for (a) wafer No. 1 and (b) wafer No. 2.

HILOE structure, and thus the HJ ideality factor is also substantially improved. This conclusion is consistent with both the simulation results (Sec. II) and the HPT photocurrent gain data in Sec. III A.

IV. CONCLUSION

Both numerical simulations and experimental results have shown that the growth of a thin, low-doped N^--InP layer in the emitter of a N-InP/p^+-$In_{0.53}Ga_{0.47}As$/n-$In_{0.53}Ga_{0.47}As$ HPT can improve both its optical sensitivity and gain-bandwidth product (due to higher current gain and lower emitter-base junction capacitance) by diminishing the recombination current at the heterointerface. An improvement of current gain by a factor of 4.5 over conventional HPT structures has been achieved at an input optical power of 40 nW. The significant gain enhancement of the HILOE HPT indicates that both bulk and interface recombination currents at the emitter/base junction are the major sources of recombination for this materials system.

The HILOE structure can also be applied to other material systems (such as GaAs/AlGaAs) if a proper surface passivation technique is used which reduces the high surface recombination currents. One of the strengths of the HILOE structure is that it can diminish the recombination current by reducing the minority-carrier concentration in the notch region of the HJ, rather than by increasing the minority-carrier lifetime. Hence, the performance of the HPTs is less dependent on the quality of heterointerface growth method used.

It has been pointed out[18] that the use of a graded base can reduce the electron transit time which increases the bandwidth of the bipolar transistor. This idea has also been demonstrated successfully for the AlGaAs/GaAs HPT.[52] Another advantage of the graded base is to reduce the base[42] and surface recombination.[53] Hence, the use of double emitters (or bases) with a high-low carrier-concentration profile along with a graded base is expected to result in both a high-sensitivity, and high-bandwidth HPT.

ACKNOWLEDGMENTS

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APPENDIX: A HIGH-LOW BASE HPT (HILOB HPT)

In past work, an extra undoped, composition-abrupt base has been used as a spacer layer (called a "setback layer") to reduce the displacement of the p/n junction into the emitter region of bipolar transistors grown by MBE and metal-organic chemical-vapor deposition.[54,55] However, the low-high carrier-concentration profile in the base region has been shown to introduce excessive recombination currents in the base.[56] This can be explained by the comparison of the energy-band diagrams of a conventional HPT [Fig. 1(a)] and a low-high base HPT [Fig. 11(a)]. Here, the doping concentration (N_{A1}) and layer thickness (d) of the spacer layer are assumed to be 1×10^{16} cm^{-3} and 200 Å, respectively. Other parameters used for calculating the energy bands are the same as those used in Fig. 1(a). Note that, from Fig. 11(a), the notch region on the base side of the HJ is deeper, thereby introducing more bulk recombination. In this case, the HJ ideality factor (n) gives 1.9, whereas $n = 1.8$ for the conventional HPT.

This excessive recombination current can be eliminated simply by increasing the doping (N_{A1}) in the spacer layer beyond the doping density in the base—a high-low base HPT (HILOB). The energy-band diagram of this structure is shown in Fig. 11(b), where $N_{A1} = 2\times10^{18}$

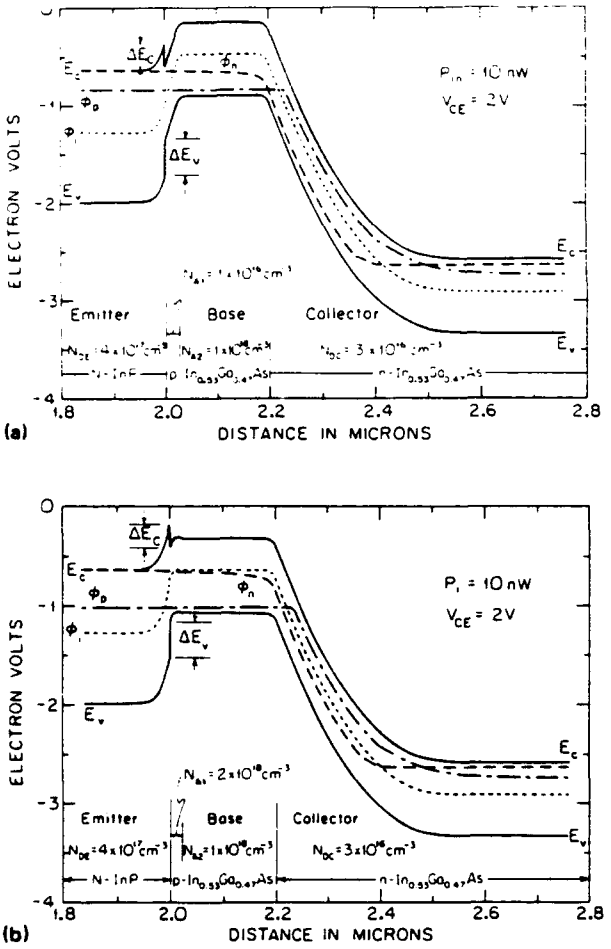

FIG. 11. Calculated energy-band diagrams of the (a) low-high base and (b) high-low base HPTs. In (a), the doping concentration (N_{41}) and layer thickness (d) of the spacer layer were assumed to be 1×10^{16} cm^{-3} and 200 Å respectively. In (b), $N_{41}=2\times10^{18}$ cm^{-3} $d=200$ Å were assumed.

cm^{-3}, $d=200$ Å were assumed. Here, the notch region is reduced, and the calculated HJ ideality factor (n) is 1.05. Note that a built-in potential exists in the base region which can accelerate electrons through the base.

Thus, a HILOB HPT as well as a HILOE HPT can both improve the photocurrent gain and gain-bandwidth product at low input optical power. The insertion of a heavily doped base layer reduces the base resistance, and thus it does not degrade the frequency response at high input optical power. On the other hand, the emitter-base capacitance (C_E) is larger than that of the HILOE HPT, leading to a larger emitter charging time.

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D. $In_{0.53}Ga_{0.47}As/InP$ heterojunctions with low interface defect densities

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Interface charge densities and conduction-band offset energies for liquid-phase epitaxially grown *n*-N isotype $In_{0.53}Ga_{0.47}As/InP$ heterojunctions have been measured using capacitance-voltage methods. Extremely low interface charge densities have been obtained in some samples, and they are found to be independent of both the measurement temperature and the magnitude of lattice mismatch. Our samples show a clear peak and notch in the apparent free-carrier concentration profile at temperatures as low as 83 K. This is in contrast to results reported previously where the notch, due to the carrier depletion at the heterojunction, was observed to vanish at low temperature. An electron trap has been identified in one of the samples. The trap is uniformly distributed within the bulk of the $In_{0.53}Ga_{0.47}As$ layer at a density of 5×10^{14} cm^{-3}. In spite of the presence of this relatively low density defect, the heterojunctions grown for this study apparently have considerably lower interface defect densities than observed by others.

I. INTRODUCTION

Heterojunctions (HJ) in the lattice-matched InP-based material system have long been used in optoelectronic devices. In addition to their conspicuous advantages in applications for fiber optical communications, InP-based HJ bipolar transistors (HBTs) with cutoff frequencies of over 100 GHz have been reported.[1] The high performance of these devices relies on good heterointerface characteristics: i.e., low defect densities and sharp interfaces. Numerous efforts have been made toward developing optimum conditions to grow high-purity InP and lattice-matched $In_{0.53}Ga_{0.47}As$ epitaxial layers.[2-10] However, little attention has been paid to the heterojunction interface properties in terms of growth conditions. Nevertheless, up to now, measurements[11-14] have shown that there is a high density of traps accumulated at the $In_{0.53}Ga_{0.47}As/InP$ heterointerface. The localized traps usually have densities about one order of magnitude higher than the free-carrier concentration in the semiconductor bulk region. This high interface defect density affects the electrical properties of devices where carriers are transported across the heterointerface. Furthermore, it is found that the deep traps can modify the shape and height of the energy barrier[11-16] at the HJ.

It is generally thought that the main factors which affect the HJ properties are (1) lattice mismatch at the heterointerface and (2) the source material purity. However, the effects on the HJ properties arising from these two factors are still unclear. Ogura[12] suggested that the high density of localized charge at $In_xGa_{1-x}As/InP$ HJs[17] was due to defects induced by lattice mismatch. Photoluminescence (PL) studies[18-20] showed that the spectra of lattice-mismatched $In_xGa_{1-x}As/InP$ HJs either (i) exhibit a low energy, broad peak, or (ii) the PL exciton peak full width at half maximum is strongly correlated to the magnitude of the lattice mismatch. Hall measurements[20,21] of $In_xGa_{1-x}As/InP$ HJs also showed that the electron mobility of the $In_xGa_{1-x}As$ was strongly affected by the lattice mismatch. However, recent studies on lattice-mismatched InGaAs/GaAs HBTs[22] have shown that charge recombination at lattice-mismatched HJs is insignificant, and the time-independent current gain is not affected by the lattice mismatch.

On the other hand, the source materials purity issue has long been ignored. For liquid-phase epitaxy (LPE), long source baking time is often used to achieve low doping concentrations and high carrier mobilities. Indeed, Pan *et al.*[10] have shown recently that the starting In purity is the main factor that determines the background doping concentrations and mobilities of the epitaxial layers. Nevertheless, to date there are no reports where the effects of source material purity on HJ interfaces has been quantitatively determined.

It is the purpose of this work to identify the origin of the interface defects. This paper presents, to our knowledge, the first complete and systematic study of the influence of both lattice mismatch and material purity related defect levels on the heterojunction diffusion potential.

The discussion is organized as follows: In Sec. II we give a detailed description of sample preparation with particular emphasis on the epitaxial growth conditions. In Sec. III, we study the effects of lattice mismatch on the $In_xGa_{1-x}As/InP$ HJ system. In conjunction with the organic-on-inorganic semiconductor contact method, capacitance-voltage (C-V) measurements for LPE-grown $In_xGa_{1-x}As/InP$ HJs are studied as a function of temperature. Dependence of the measured conduction-band offset energy, interface charge density, Hall mobility, and photoluminescence spectrum on lattice mismatch are studied. In Sec. IV, we present measurements on the effects of source material purity on $In_xGa_{1-x}As/InP$ heterointerfaces. There, C-V data are studied as a function of temperature and measurement frequency. Deep-level transient spectroscopy (DLTS) is used to determine the characteristics of the traps in the bulk and at the heterointerface. Computer simulations

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of the apparent free-carrier concentration profiles are then used to analyze the experimental results at several temperatures. Finally, in Sec. V, conclusions are presented.

II. SAMPLE PREPARATION

Eight LPE-grown HJ samples (Nos. 1–8) were prepared for study. The InP and $In_xGa_{1-x}As$ layers were grown on either (100) semi-insulating Fe-doped InP substrates (sample Nos. 4–6) or (100) S-doped n^+-InP substrates with an electron concentration of approximately 3×10^{18} cm^{-3}. Prior to growth, the substrates were organic solvent cleaned and etched in a solution of 3:1:1 H_2SO_4:H_2O_2:H_2O for 4 min, and then rinsed in deionized water immediately before loading into a graphite boat. The growth solutions for the $In_xGa_{1-x}As$ layers were prepared using either ultrahigh purity,[23] 99.99999 + % In (sample Nos. 1–6), or 99.9999 + % In (sample Nos. 7 and 8) prebaked for over 24 h at 700 °C. Afterwards, 99.9999% pure polycrystalline InAs and GaAs were added to the melts. Lattice-mismatched layers of $In_xGa_{1-x}As$ were grown by varying the atomic percentage of Ga in the solution. The solution was baked prior to growth at 20 °C higher than the liquidus temperature for more than 48 h to reduce the background doping concentrations of the layers. The In-InP solution for the InP buffer layer was prepared using prebaked In (99.99999 + % for sample Nos. 1–3, and 99.9999 + % for sample Nos. 7 and 8). The solution was then baked for an additional 48 h after adding a small amount of InP for saturation purposes. Surface preservation during heat-up and melt homogenization was achieved by keeping the substrate under a Sn-InP melt[24] using a basket inserted into the graphite boat. Furthermore, the substrate was either placed under an unsaturated In-InP melt for 5 s, or simply slid through the melt just before growth to obtain a fresh, melted back surface. We found that there was no difference between these two methods in terms of material quality. However, the grown layer surface was much smoother when employing the slide-through method.

For sample Nos. 1–3, 7, and 8, a 2–3-μm-thick InP buffer layer was then grown by the two-phase method[25] at a rate of 0.2 μm/°C, followed by an $In_xGa_{1-x}As$ layer grown by 3 °C of supercooling at 647 °C. The $In_xGa_{1-x}As$ layers of sample Nos. 4–6 were directly grown on InP substrates without buffer layers for Hall-mobility measurements. Care was taken to get a uniform and smooth surface morphology. For this purpose, the furnace was calibrated to obtain a uniform temperature profile to within $\pm$ 0.1 °C over a 25-cm length. Table I lists all the growth and materials data for the samples studied in this work. Double-crystal x-ray diffraction was used to determine the lattice mismatch, $(\Delta a/a)_\perp$, between the $In_xGa_{1-x}As$ layer and the underlying InP layer. Here, (004) was used as the x-ray reflection plane. The values of lattice mismatch of the eight samples studied are also listed in Table I. Here $(\Delta a/a)_\perp < 0$ indicates that the $In_xGa_{1-x}As$ layer is under compressive strain with respect to the InP layer at room temperature.

To facilitate the *C-V* measurements, organic-on-inorganic (OI) diodes were fabricated to form a rectifying contact with the top $In_xGa_{1-x}As$ layer (see inset, Fig. 1). These diodes were made in the following manner:[26,27] A 2000-Å-thick In layer or a 100-Å Cr with 2000-Å Au layer were vacuum deposited to form the back contact to the InP substrate. This was followed by vacuum sublimation of a 1000-Å-thick layer of the prepurified organic semiconductor onto the epitaxial surface of the wafer. The organic compound employed was 3, 4, 9, 10 perylenetetracarboxylic dianhydride (PTCDA). Finally, circular In contacts of area 5.3×10^{-4} cm^2 were deposited through a shadow mask onto the PTCDA surface to form an ohmic contact with the organic layer. The organic layer forms a rectifying HJ barrier with the underlying semiconductor such that large reverse-bias voltages can be applied to the diode (typically 18 V for $In_{0.53}Ga_{0.47}As$ with a doping of 1×10^{15} cm^{-3}) without inducing large reverse-bias leakage currents. Usually, the reverse saturation current is less than 10 mA/cm^2, and thus the sample under study can be deeply depleted prior to undergoing breakdown. A detailed description of the technique of using organic films for wafer analysis has been presented elsewhere.[26,27]

III. LATTICE-MISMATCH EFFECTS

Sample Nos. 1–6 were grown for the purpose of studying the effects that lattice mismatch have on the heterointerface. Sample Nos. 1–3 were grown on n^+-InP substrates with an undoped InP buffer layer and were used for *C-V* and PL measurements, while sample Nos. 4–6 were grown directly on semi-insulating Fe-doped InP substrates for Hall

TABLE I. Growth and materials data for samples studied.

Sample No.	1	2	3	4	5	6	7	8
$(\Delta a/a)_\perp$[a]	−0.03%	−0.24%	+0.26%	−0.06%	−0.25%	+0.18%	−0.02%	−0.06%
Substrate	n^+	n^+	n^+	SI	SI	SI	n^+	n^+
In source	99.99999% +	99.99999% +	99.99999% +	99.99999% +	99.99999% +	99.99999% +	99.9999% +	99.9999% +
InP N_D	2.6×10^{15}	3.2×10^{15}	3.4×10^{15}				1.6×10^{16}	1.2×10^{16}
$In_xGa_{1-x}As$ N_D	8.9×10^{14}	1.3×10^{15}	2.3×10^{15}	1.2×10^{15}	1.4×10^{15}	1.6×10^{15}	5.2×10^{15}	6.5×10^{15}

[a]Values were obtained by averaging six x-ray measurement points across a 15 × 15-mm^2 wafer. The variation of lattice mismatch across the wafer is less than ± 5%.

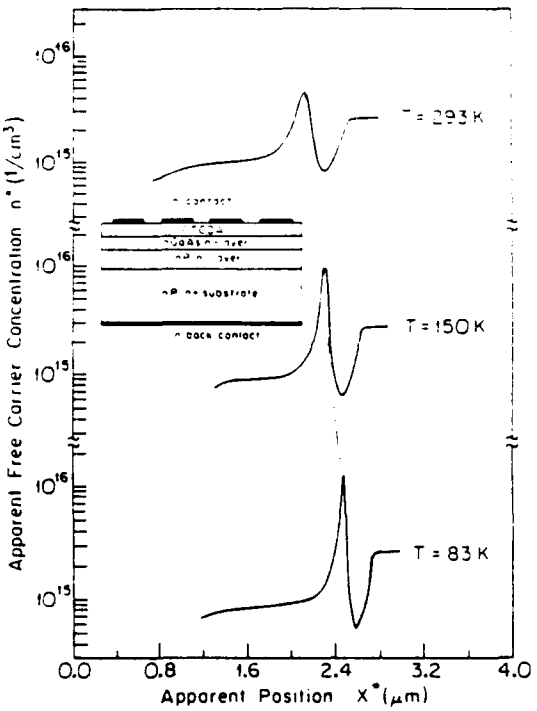

FIG. 1. Apparent free-carrier concentration $n^*(x^*)$ profiles of sample No. 1 at several temperatures. The inset shows the organic-inorganic diode structure used in this work.

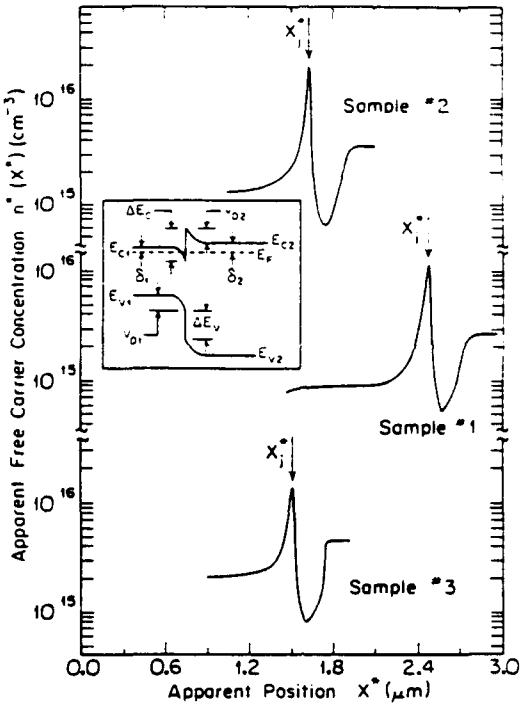

FIG. 2. Measured apparent free-carrier concentration profiles for sample Nos. 1–3 at 83 K. The inset shows the energy-band diagram of a typical type-1 heterojunction.

measurements. All these samples were grown using an ultra-high-purity In source to eliminate defects introduced by the source material. The magnitude of the lattice mismatches for the samples are indicated in Table I.

A. *C-V* measurements

The apparent free-carrier concentration profiles $[n^*(x^*)]$ for sample No. 1 measured at several temperatures are shown in Fig. 1. The measurement frequency was 1 MHz, and the amplitude of the ac signal was 10 mV_{rms}. As shown in the figure, the peak and notch which correspond to majority-carrier accumulation and depletion at the heterointerface, respectively, are clearly evident at all temperatures. No distortion was observed as the temperature was varied between 293 and 83 K except that the peak in $n^*(x^*)$ shifts toward the substrate (x_j^* increasing) as the temperature is decreased. It can be shown that the profile shift is largely due to series resistance and surface states existing at the rectifying contact.[28] The apparent free-carrier concentration profiles of sample Nos. 2 and 3 also exhibit a behavior similar to sample No. 1 at all measurement temperatures. The apparent free-carrier concentration profiles for sample Nos. 1–3 at 83 K are shown in Fig. 2. These results contradict the suggestion of Lang *et al.*[29] that the HJ series resistance causes the notch in the $In_{0.53}Ga_{0.47}As/InP$ HJs to vanish at low temperature. According to that assumption, all low-temperature *C-V* measurements made for this HJ system should show the same distortion, which is clearly contrary to our results.

To interpret the free-carrier concentration profiles in Figs. 1 and 2, we show the band diagram of an *n*-N isotype type-1 HJ such as $In_{0.53}Ga_{0.47}As/InP$ in the inset of Fig. 2. The conduction-band offset energy is related to the HJ diffusion potential (V_{DK}) via

$$\Delta E_c = qV_{DK} + \delta_1 - \delta_2. \tag{1}$$

Here, q is the electronic charge, and δ_1 and δ_2 are the depths of the Fermi levels as measured from the conduction-band edges in the large- and small-band-gap layers, respectively.

A simple capacitance-voltage (*C-V*) technique to determine the band offset and fixed interface charge density of HJs using $n^*(x^*)$ profiles was proposed by Kroemer *et al.*[30] They showed that the diffusion potential of an *n*-N isotype HJ can be found by determining $n^*(x^*)$ at apparent position x^* in the heterointerface region, and using

$$V_{DK} = \frac{q}{\epsilon}\int_{-\infty}^{\infty} [N_D(x^*) - n^*(x^*)](x^* - x_j)dx^*. \tag{2}$$

The fixed charge density at the HJ, σ, can also be determined via

$$\sigma = -\int_{0}^{\infty} [N_D(x^*) - n^*(x^*)]dx^*, \tag{3}$$

where ϵ is the semiconductor permittivity, and $n^*(x^*)$ is determined using standard *C-V* analysis methods.[31] Also, $N_D(x^*)$ is the background doping concentration which is equal to $n^*(x^*)$ far from the HJ, and x_j is the actual distance of the HJ from the rectifying contact. Here, the peak in $n^*(x^*)$ is located very close to x_j, although shifts in the profile due to series resistance and surface states such as those in Fig. 1 can lead to errors in determining x_j. Once the diffusion potential is determined from Eq. (2), the conduction-band offset can then be obtained using Eq. (1).

The low and flat free-carrier concentrations obtained on both sides of the HJ provide an accurate determination of the background free-carrier concentration (N_D), thus minimizing the error in calculating the diffusion potential, V_{DA}, and hence the conduction-band offset energy, ΔE_c, using Eqs. (1) and (2). The *measured* conduction-band offset energy as a function of temperature for sample Nos. 1–3 are shown in Fig. 3. The error bars are due to the small uncertainties in determining x_i and the background doping (N_D) on the $In_xGa_{1-x}As$ side of the heterojunction. The nonuniformity of the background doping concentration on the $In_xGa_{1-x}As$ side ($\pm 2\times10^{14}$ cm^{-3}) gives an error of about ± 6 meV in calculating the apparent conduction-band offsets. It is clear that the measured conduction-band energy discontinuities for sample Nos. 2 and 3 are indistinguishable from those of sample No. 1, although $(\Delta a/a)_\perp$ is as large as 0.26% for the later samples. According to Kuphal,[32] there should be a 24-meV difference between the band-gap energies of the $In_xGa_{1-x}As$ layers of sample Nos. 2 and 3 due to their compositional difference. This corresponds to about a 10-meV difference in conduction-band offset values, if we use the 40:60 ratio in dividing the $In_xGa_{1-x}As$ and InP band-gap difference between the conduction and valence bands.[26] This variation in ΔE_c, however, is within the limit of measurement error.

The measured conduction-band offset energy is clearly independent of temperature, and has an average value of (0.22 ± 0.02) eV, consistent with room-temperature values reported previously for $In_{0.53}Ga_{0.47}As$/InP HJs.[11-14,29] Apparently, this is the first time that ΔE_c measured using *C-V* techniques for this HJ system is found to be temperature independent.

A good indication of the heterointerface quality is the density of the fixed charges which reside at heterointerface. The dangling bonds and defects caused by the lattice mismatch, *if* they are electrically active, should trap free carriers and create fixed interface charges. Figure 4 shows the interface fixed charge density as a function of temperature for these three samples. It can be seen that sample No. 3, which has the largest $(\Delta a/a)_\perp$, also has the smallest σ, while sample No. 1, which is lattice matched at the growth temperature, has the largest σ. It should also be noted that the interface charge densities for these samples are at least one order of magnitude smaller than values reported previously for $In_{0.53}Ga_{0.47}As$/InP HJs,[11-14] and are at values approaching the limit of accuracy of the *C-V* measurement technique. Furthermore, the lattice-mismatch values for sample Nos. 2 and 3 are at least twice as large as those studied previously.[12,13] This result is evidence that there is no correlation between interface defect density and lattice mismatch for high-quality $In_xGa_{1-x}As$/InP HJs, at least for $|(\Delta a/a)_\perp| < 0.26\%$. In fact, this is the maximum range that the $In_xGa_{1-x}As$ layer can be grown on InP by LPE without inducing serious surface nonuniformities.

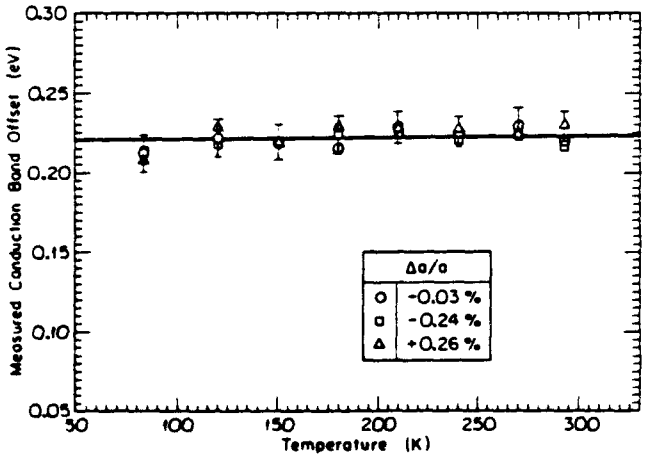

FIG. 3. Measured conduction-band offset energies for sample Nos. 1–3 as a function of temperature.

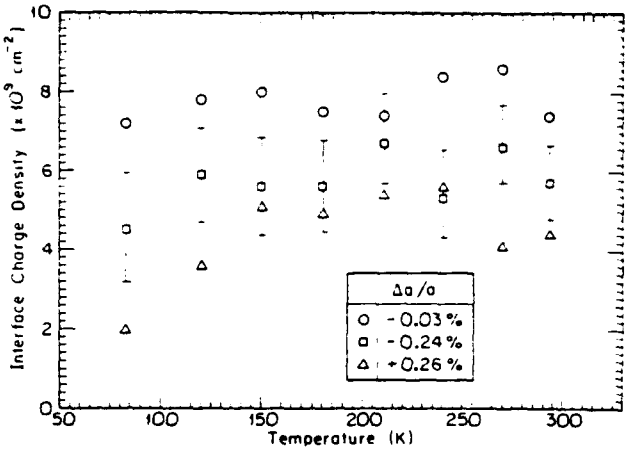

FIG. 4. Measured interface charge densities of sample Nos. 1–3 as a function of temperature.

B. Photoluminescence studies

The nonradiative recombination and other optical properties of the lattice-mismatched layers were investigated using photoluminescence. Photoluminescence from the $In_xGa_{1-x}As$ layers was excited using an Ar-ion laser, with the excitation power intensity varied from 0.5 to 15 W/cm^2 using neutral density filters. The light was chopped and analyzed with a 0.75-m double-grating monochromator and Ge detector connected to a lock-in amplifier. All the spectra were taken at 20 K.

The spectra obtained with an excitation power intensity of 0.5 W/cm^2 for sample Nos. 1–3 are shown in Fig. 5. Increasing the power intensity does not change the shape of the spectra. However, due to the superlinear increase of the exciton peak intensity with respect to excitation power, detail in the low-energy portion of the spectra is obscured at high power. The exciton linewidths are from 5 to 6 meV, and are not affected by the magnitude of the lattice mismatch. In fact, sample No. 2 shows the highest exciton peak intensity and narrowest linewidth, which is about 4.7 meV. This result is contrary to the data of Su *et al.*,[20] which show a linewidth increasing from 8 to 23 meV as $(\Delta a/a)_\perp$ changes from 0% to -0.25%. We suspect that the change of linewidth in the data of Su *et al.* is due to the increasing background doping concentration with increasing lattice mismatch in their sam-

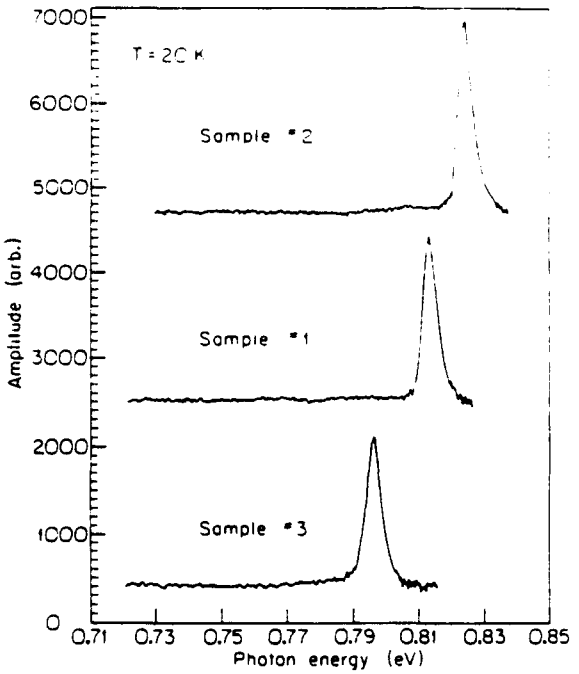

FIG. 5. Photoluminescence spectra of sample Nos. 1–3 at 20 K. The excitation power intensity is 0.5 W/cm^2.

ples. The spectra in Fig. 5 also show no additional peaks within 90 meV of the exciton peak energies. This result again contradicts previous studies,[18,19] where a broad peak arising from midgap states attributed to lattice mismatch was observed. We point out that the $In_xGa_{1-x}As$ layer thicknesses of sample Nos. 2 and 3 are about 1.5 μm, which is in the range for which Yagi[18] showed that the broad peak had the maximum intensity. If this feature was in fact due to lattice mismatch, then it should be universally observed in the PL spectra. However, no trace of this broad peak can be observed in our samples, even though the magnitude of the lattice mismatch is about twice as large as the samples studied by Yagi.[18] These optical measurements support our electrical measurements (C-V and Hall measurements, described below) in that the energy levels created by the lattice mismatch and its related defects do not reside in the band-gap region. Therefore, the HJ interface properties are not affected by the lattice mismatch for this HJ system.

C. Hall measurements

Sample Nos. 4–6 were grown on semi-insulating Fe-doped (100) InP substrates for Hall measurements. Sample Nos. 4 and 5 have a lattice-mismatch value comparable to sample Nos. 1 and 2, respectively (see Table I). However, we have not been able to grow an $In_xGa_{1-x}As$ layer with a positive lattice mismatch greater than 0.2% on semi-insulating InP substrates. The magnitude of the lattice mismatch of sample No. 6 is thus smaller than for sample No. 3, but qualitative comparison can still be made.

Hall measurements were made using a standard van der Pauw configuration with ohmic contacts placed on four corners of a 10 mm × 10 mm square wafer. The ohmic contact diameter was $\sim$ 0.5 mm. Thus, the error induced by the contact size effect is less than 1%. The magnetic field intensity used was 2500 G. We used a small ac signal as the current source to eliminate misalignment and Ettingshausen–Seebeck effects.[4] The magnitude of the ac current applied was $\leq 50\,\mu A_{rms}$. Table II lists the Hall mobility values and carrier concentrations for these three samples at both room temperature and 77 K. We see that the room-temperature and 77-K Hall mobilities for these samples are all above 11 000 and 44 000 cm^2/V s, respectively. These are among the highest values ever reported for LPE-grown $In_xGa_{1-x}As$ layers in a doping range comparable to the samples studied here. The compensation ratios $[(n_{300\,K} - n_{77\,K})/n_{300\,K}]$ are all within 10%. Most significantly, there is no apparent relationship between the Hall mobility value and the magnitude of the lattice mismatch.

According to Matthews,[35] the critical thickness for which misfits can be accommodated by strain alone is about 520 Å for samples with mismatches as large as sample Nos. 2 and 3. However, the actual $In_xGa_{1-x}As$ layer thicknesses for these samples are about 1.5 μm, which are much thicker than this critical value. Therefore, misfit dislocations must occur at or near the HJs to accommodate part of the strain. The estimated dislocation line density is about 10^5 cm^{-1}.[36] That is, more than 90% of the misfit is released in the formation of dislocations. The dangling bonds at the HJ interface are thus in the 10^{12} cm^{-2} range.[37] However, from the above experimental results, we find that there is almost no difference caused by lattice mismatch in either the electrical or optical measurements. Thus, we can conclude that the states created by misfit dislocations are not electrically active. The energy states related to lattice mismatch are pulled into either the conduction or valence band at the heterointerface, instead of residing in the band-gap region.

III. SOURCE MATERIAL PURITY EFFECTS

As we have shown above, lattice mismatch does not play a significant role in determining the HJ interface properties. Therefore, sample Nos. 7 and 8, which were grown with a less pure In source than the other six samples, were used to study source material effects on the HJ properties. Frequency-dependent capacitance-voltage measurements and deep-level transient spectroscopy (DLTS) were performed on these latter samples to further investigate the source of interfacial defects observed in previous work.

TABLE II. Mobilities and carrier concentrations for sample Nos. 4, 5, and 6 at room temperature and 77 K.

Sample No.	6	7	8
μ_{300} (cm^2/V s)	11 800 ± 200	11 400 ± 200	11 100 ± 200
μ_{77} (cm^2/V s)	45 300 ± 300	44 900 ± 300	44 200 ± 300
n_{300} (cm^{-3})	1.2×10^{15}	1.4×10^{15}	1.6×10^{15}
n_{77} (cm^{-3})	1.1×10^{15}	1.3×10^{15}	1.4×10^{15}

A. *C-V* measurements

As for the lattice-mismatched samples, the apparent free-carrier concentration profiles for sample No. 7 show no distortion at temperatures as low as 95 K, and the measured conduction-band offset energies remain constant with temperature. Although the length of solution baking time and growth conditions are the same for all the samples, the background doping concentrations for both InP and $In_xGa_{1-x}As$ layers of sample No. 7 are at least four times higher than for the samples grown with the high-purity In source. More important, however, is that the interface fixed charge density of sample No. 7 is at least five times higher than for sample No. 1, and one order of magnitude higher than for sample No. 3, as shown in Fig. 6. Again, no temperature dependence for the interface charge density is observed.

The behavior of the apparent free-carrier concentration profiles is somewhat different for sample No. 8, as shown in Fig. 7. Here, the profiles also display a clear peak (peak A) and notch at high temperature. However, a second peak (peak B) emerges in the notch region at $T \lesssim 110$ K that is not observed in the other samples. This peak grows as the temperature decreases, while peak A shrinks. The relative growth and shrinkage of these two peaks is due to charge transfer from the HJ accumulation region (peak A) into the trap sites (peak B) at low temperature. The multiple-peak feature has also been observed by Jeong *et al.*[38] for InGaAs/GaAs HJs, and Andre *et al.*[39] and Leu and Forrest[15] for $In_{0.81}Ga_{0.47}As$/InP HJs.

The appearance of such a sharp peak in the notch region suggests that either the trap energy or its spatial distribution is very narrow in this sample. As we discuss below, DLTS studies indicate that the trap is almost uniformly distributed across the bulk of the $In_xGa_{1-x}As$ layer. Thus, we can rule out the possibility that the sharp peak is a result of a spatially confined trap level at the heterointerface, but rather is due to a narrow trap energy distribution. In *C-V* measurements, the apparent position (x^*) is a function of the bias voltage, and as such the apparent position is related to the depth of the Fermi energy at the edge of the depletion region. The

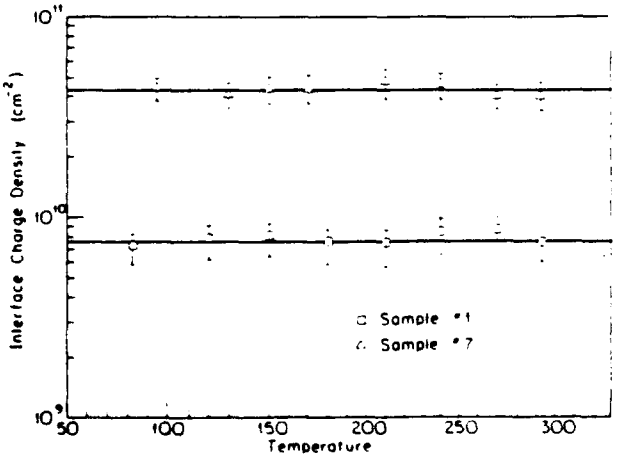

FIG. 6. Measured interface charge density for sample No. 7 at different temperatures. Values for sample No. 1 are also shown as a comparison.

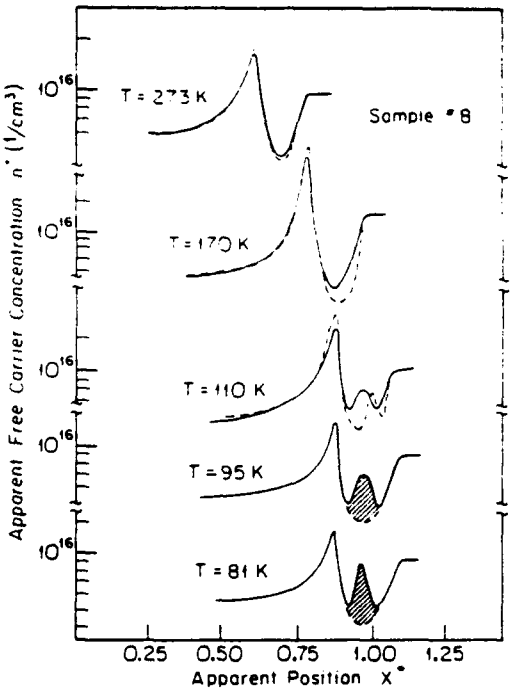

FIG. 7. Apparent free-carrier concentration profiles of sample No. 8 at different temperatures. The solid lines represent the experimental data, and the dotted lines show the computer-simulated results.

trapped electrons are thermalized as the applied bias voltage pulls the quasi-Fermi level below the trap energy level. Thus, the apparent spatial sharpness of the second peak in the $n^*(x^*)$ profile indicates that the width of the trap energy distribution is very narrow. A precise estimate of this energy-level width, however, is not possible due to the Debye length limitations to the resolution of the *C-V* data.[40]

We have also investigated the frequency dependence of $n^*(x^*)$ of sample No. 8 at 2 MHz, 1 MHz, 400 kHz, and 200 kHz. In order to maintain consistency during the measurement, a 10-mV$_{rms}$ test signal was used at all frequencies. Figure 8 shows $n^*(x^*)$ at 81 K for three different measurement frequencies, where it is observed that the notch depth is independent of frequency, except that the position of the peaks associated with the trap (peak B) and with carrier accumulation (peak A) shift toward the substrate as frequency increases. This result is different to a previous report[14] where the notch totally disappears below 123 K, and at measurement frequencies as low as 100 kHz. This discrepancy can be attributed to differences in trap energy and spatial distribution between our samples and those studied elsewhere. The data obtained from DLTS measurements, which we discuss below, show the trap in sample No. 8 is uniformly distributed in the bulk region, and has an energy level much shallower than the one observed by Kazmierski *et al.*[14] Thus the frequency dependence of the data for sample No. 8 is not as pronounced as that in Ref. 14.

The apparent conduction-band offset of sample No. 8 measured as a function of temperature and frequency using Eqs. (1) and (2) is shown in Fig. 9(a). The apparent band

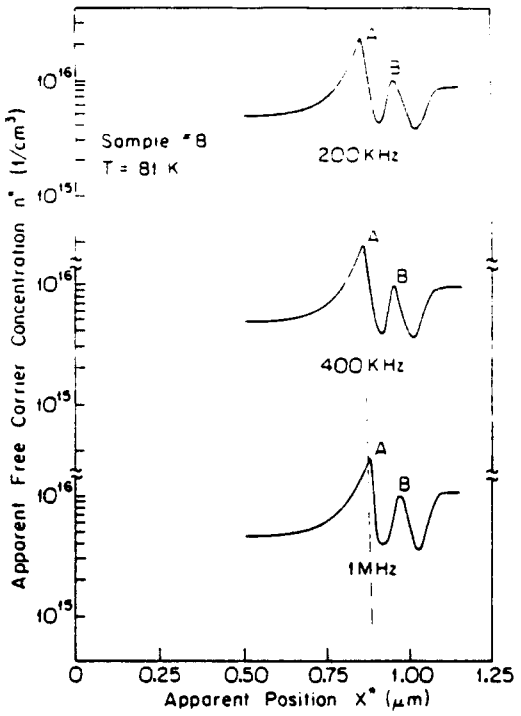

FIG. 8. Apparent free-carrier concentration profiles of sample No. 8 for three different testing frequencies at 81 K.

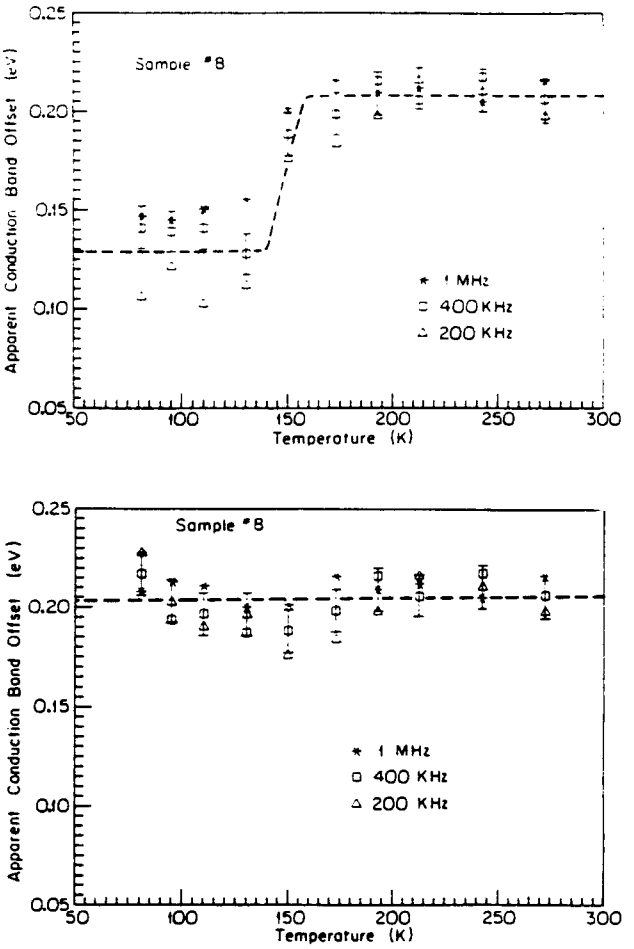

FIG. 9. (a) Measured conduction-band offsets as a function of temperature for sample No. 8 obtained using the depletion capacitance-voltage method. (b) Measured conduction-band offset for sample No. 8 after correction using Eq. (4).

offset energy stays almost constant down to about 150 K. As temperature is lowered further, ΔE_c starts to drop and becomes flat again at $T < 120$ K. Contrary to previous results,[11] no frequency dependence of the transition in the value of ΔE_c is observed when temperature is varied.

It should be noted, however, that the apparent conduction-band offset measured at low temperature is not equal to the actual offset energy (ΔE_c) since the apparent offset energy was obtained by incorrectly applying Eqs. (1) and (2) under conditions where a second, trap-related peak is clearly evident. It has been shown[16] that Eqs. (1) and (2) can only be accurately applied under conditions of low trap density where the potential due to trapped charge is small compared with the heterojunction dipole potential. This difficulty can be removed by using[16]

$$V_D(0) = V_{DA} + \frac{q}{\epsilon}\int_{x_i}^{x} N_T^*(x^*)(x^* - x_i)dx^*, \quad (4)$$

where $V_D(0)$ is the diffusion potential due to the *intrinsic* HJ dipole found by subtracting the contribution of trapped charges using the integral in Eq. (4). Here, N_T^* is the apparent trap density at position x^*. It is important to note that in deriving Eq. (4), N_T^* is not necessarily assumed to be due to an interface trap: it could also be due to a bulk trap. For sample No. 8, $N_T^*(x^*)$ can be obtained by subtracting the trap contribution (peak B) from an *assumed* smoothly curved notch in the $n^*(x^*)$ profile, i.e., the cross-hatched region in the curves in Fig. 7 at $T = 81$ K and $T = 95$ K (for clarity, cross-hatching is omitted for the 110-K curve). Both N_T^* and $x^* - x_i$ are positive, such that the integral in Eq. (4) is also positive in this case. Therefore, the corrected diffusion potential, $V_D(0)$, and hence the actual conduction-band offset energy, will be larger than the values plotted in Fig. 9(a) as temperature is decreased. Figure 9(b) shows the conduction-band offset energies obtained using Eq. (4). As shown in this figure, the measured conduction-band offset energy at low temperature is the same as that measured at high temperature to within $\pm$ 15 meV.

B. DLTS measurements

In order to investigate the source of the different behavior of sample Nos. 7 and 8, DLTS measurements have been performed on these two wafers. The various material layers were characterized by applying different steady-state reverse-bias voltages to the OI diodes. The majority-carrier pulse height was 3 V, and the pulse duration was 500 μs corresponding to the minimum pulse duration that saturates the capacitance transient. In the temperature range from 330 to 90 K, only one deep level was detected on the $In_xGa_{1-x}As$ side of the HJ of sample No. 8, and no trap was detected in sample No. 7.

The emission rate of the trap in sample No. 8 was determined by fitting the slope of $\ln\{1-[C(t)/C_0]\}$ versus time, where $C(t)$ is the capacitance at time t from the end of the majority-carrier excitation pulse, and C_0 is the steady-state capacitance taken at $t \to \infty$. The decrease of the initial value of capacitance with respect to its steady-state value indicates that this is a majority-carrier (electron) trap level.

Figure 10 shows the emission rate [plotted as $\ln(e_n/T^2)$] versus q/kT for sample No. 8. Here k is Boltzmann's constant, and e_n is the trap emission rate. The error bars in this figure are due to randomness in the measured value of C_0 (± 0.1 pF). The trap energy determined from the slope of the plot is (0.10 ± 0.02) eV below the conduction-band minimum, which is similar to the trap reported previously by Whitney *et al.*[13] for LPE-grown $In_{0.53}Ga_{0.47}As$.

The spatial distribution of the traps was determined by applying different magnitudes of steady-state reverse-bias voltages and majority-carrier saturation pulse heights. The trap concentration was then found using:[41]

$$N_t(x) = 2\{[C_0 - C(0)]/C_0\}N_D, \qquad (5)$$

where $C(0)$ is the capacitance at $t = 0$. The trap is found to be uniformly distributed in the bulk region at a density of $N_t = (5 \pm 2) \times 10^{14}$ cm^{-3}. This value is consistent with previously reported data for $In_{0.53}Ga_{0.47}As$/InP HJs grown with 99.9999 + % pure In.[11,13] However, trap accumulation at the heterointerface which was commonly observed in previous studies does not appear in our sample. In fact, we propose that the difference in the low-temperature apparent free-carrier concentration profiles between our data and previous results[11,13] are due to the lack of trap accumulation in our samples. Trap accumulation at the heterointerface depends critically on the initial growth stage of the epitaxial layers. However, due to the lack of published information on this point, we cannot make a systematic comparison between our growth technique and those used by others. Thus, we cannot ascertain the direct cause of the growth-induced differences between all of the samples reported in the literature.

Using DLTS data obtained for this trap, computer simulation was used to analyze the $n^*(x^*)$ profiles of sample No. 8. The calculation method used was a solution of Poisson's equations in the HJ region based on the model proposed by Whiteway.[42] The basic assumptions of the model are that the reverse-bias current through the rectifying barrier is vanishingly small, and that the quasi-Fermi level is flat throughout the depletion region. The parameters used in the calculation were obtained from experiment, and are listed in Table III. The trap activation energy (E_t) was the only adjustable parameter. The simulated profiles are shown by the dotted lines in Fig. 7. The simulated profiles are observed to fit the experimental data at 273 K. However, discrepancies between the data and the calculation which appear in the notch region at lower temperature are believed to be due to compositional gradients near the heterointerface, which are not included in the model. That is, the shallower notch for the measured profiles indicate that the band bending on the InP side of the HJ is smaller than that assumed for the calculated profiles, where the heterointerface is assumed to be abrupt. The very high density of free carriers accumulated on the $In_xGa_{1-x}As$ side of the HJ makes the band bending less sensitive to composition gradients in this region. Therefore, almost all the discrepancies between measurement and simulation occur on the depleted (InP) side. This effect is even more pronounced at low temperatures as the Fermi level moves closer to the conduction-band edge, and hence there are even more electrons accumulated at the $In_xGa_{1-x}As$ side of the junction. Nevertheless, these simulated profiles clearly reveal the general features of the measured results. The best fits to the apparent free- carrier concentration profiles were obtained by taking $E_t = 85$ meV, which is within the limits of error for the DLTS result of (100 ± 20) meV.

The difference between sample Nos. 7 and 8 is due to the manner in which the defects are distributed during growth. In sample No. 8, the defects are confined in a very narrow energy range in the bulk region, resulting in a sharp peak in the apparent free-carrier concentration profile. The defects in sample No. 7 near the heterointerface, however, are dis-

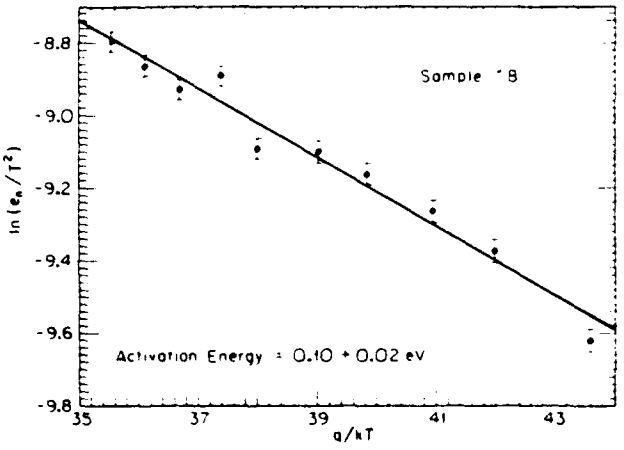

FIG. 10. Trap emission rate as a function of temperature for sample No. 8. The activation energy obtained from the slope of this plot is (0.10 ± 0.02) eV. The error bars are due to the uncertainty in choosing C_0 values.

TABLE III. Material parameters used in simulation for sample No. 8.

Conduction-band discontinuity energy (ΔE_c)	0.22 eV
Organic-inorganic semiconductor contact barrier height (V_{bi})	0.45 eV
Doping concentration ($In_xGa_{1-x}As$)	$(6 \pm 1) \times 10^{15}$ cm^{-3}
Doping concentration (InP)	$(1.2 \pm 0.1) \times 10^{15}$ cm^{-3}
Donor energy level ($E_c - E_t$)	6 meV
Trap density (N_t)	5×10^{14} cm^{-3}

persed into a wider energy distribution, resulting in a broader, unresolved peak in the apparent free-carrier concentration profile. The distribution coefficients of different impurity species might play an important role in determining the final results. However, the growth conditions which favor either bulk or interface defects are still unclear at this point.

The importance of source material purity on the HJ interface properties is quite apparent in comparing results for sample Nos. 7 and 8 to the other lattice-mismatched but high-purity samples we have studied. The source material not only affects the epitaxial layer background carrier concentration, but also the interface charge densities are dramatically reduced by employing high-purity In sources. We conclude that the relatively high HJ interface charge densities in sample Nos. 7 and 8, as well as those observed in previous studies,[11-13] are due to the impurities introduced by the less pure source materials. Furthermore, we see that even the very low bulk trap density in sample No. 8 can result in a severely distorted apparent free-carrier concentration profile in the HJ region.

IV. CONCLUSIONS

We have studied the effects of lattice mismatch and source material purity on the electrical and optical properties of $In_xGa_{1-x}As/InP$ HJs. Extremely low interface defect densities have been obtained for samples grown using ultrahigh-purity In source melts. The interface defect density is found to be independent of both the magnitude and the sign of the lattice mismatch, contrary to assertions made in previous work.[12,13] Samples grown with lower-purity In sources either show a higher value of σ, or exhibit a distinct, trap-related peak in the apparent free-carrier concentration profiles at low temperature. Very high Hall mobilities were also obtained for samples using high-purity In sources at both room temperature and 77 K, and were found to be independent of the magnitude of the lattice mismatch. Photoluminescence spectra showed very high intensity at low excitation power for all samples, and the exciton linewidths for the $In_xGa_{1-x}As$ layers were also unaffected by the lattice mismatch.

The observed free-carrier concentration profiles obtained using C-V data differ from other reports in that the notch region associated with carrier depletion at the InP side of the HJ is clearly apparent even at temperatures as low as 83 K. The measured conduction-band offset remains constant down to low temperature, with a value of $\Delta E_c = (0.22 \pm 0.02\ \text{eV})$. This is consistent with values obtained at room temperature reported previously for this heterojunction system.[11-14,23] Apparently, this represents the first time the conduction-band offset has been measured over a wide temperature range without showing significant temperature effects.

Deep-level transient spectroscopy studies indicate that a low density of traps is found to be uniformly distributed on the $In_xGa_{1-x}As$ side of the HJ in one of the samples using 99.9999 + % In. The trap activation energy is (0.10 ± 0.02) eV, and its density is $(5 \pm 2) \times 10^{14}\ \text{cm}^{-3}$, which is less than 10% of the background free-carrier concentration. The consistency of the computer-simulated apparent free-carrier concentration profiles and experimental measurements taken over a wide temperature range also support this result. The previously reported defect is associated with In source material purity, whereas no active electronic defects have been associated with lattice mismatch in this material system.

In other related work we have used similar methods to grow $In_{0.53}Ga_{0.47}As/InP$ junction field-effect transistors (JFETs) with extremely high device output resistance.[43] This high output resistance is attributed to relatively defect-free $In_{0.53}Ga_{0.47}As/InP$ heterointerfaces, and thus low interface recombination currents. Using the results presented in this work, we can make a simple estimate of the effect of interface defects on the output resistance of such FETs. For example, a JFET with a 2-μm-long by 150-μm-wide channel with a doping concentration of $5 \times 10^{16}\ \text{cm}^{-3}$ range has a drain-to-source current (I_{DS}) of about 30 mA when the device is operated in the saturation regime. The free-carrier concentration near the heterointerface, $n = I_{DS}/(AqV_{sat})$, is therefore about $6 \times 10^{17}\ \text{cm}^{-3}$ if we assume a 100-Å channel depth and a saturation velocity of $V_{sat} = 2 \times 10^7$ cm/s.[44] Here, A is the current path cross-sectional area, which is $1.5 \times 10^{-8}\ \text{cm}^2$. Commonly observed heterointerfaces have a defect densities (N_{ss}) of about $10^{11}\ \text{cm}^{-2}$.[11-13] Also, the defect capture cross sections (σ_c) are typically $10^{-15}\ \text{cm}^2$.[11] In this case, the interface recombination current density, $J = nqN_{ss}\sigma_c V_{sat}$, is about 100 A/cm^2. With a 1-V increase in the drain-to-source voltage, the modulated channel length is approximately 1 μm, which results in a recombination current of about 150 μA. The output resistance is then 6–7 kΩ, which compares to our devices with output resistance of typically 30 kΩ. This suggests that N_{ss} in our samples is less than $2 \times 10^{10}\ \text{cm}^{-2}$, which is consistent with values reported in this work using 99.9999 + % purity In. Even higher output resistances are expected for JFETs grown using ultrahigh-purity In. This calculation underscores the importance in using high-purity metal sources in order that we achieve the best performance in such heterojunction devices.

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E. Optically powered arrays for optoelectronic interconnection networks

M. Govindarajan and Stephen R. Forrest

We describe a novel integrated, optically powered optoelectronic array for use in 2-D interconnection networks. We discuss a generic optoelectronic processing structure and propose two circuit schemes for realizing these interconnect arrays. It is shown that optical powering of the array pixel electronics considerably reduces the high frequency crosstalk between adjacent array elements, leading to improvements in bandwidth by >1 order of magnitude when compared with similar conventionally powered systems. Design criteria are established for determining the trade-offs between fanout and power dissipation, and factors limiting packing density in the optically powered scheme are also discussed. We also compare the performance of optically powered optoelectronic, conventional optoelectronic and all-optical systems on the basis of bandwidth, crosstalk, packing density, and functionality and find that optical powering has several advantages for use in advanced system architectures.

I. Introduction

It has been suggested that optical computing offers the advantages of parallelism, high bandwidth, and low electromagnetic interference between channels. Nevertheless, optical computing requires the development of generic stages for interconnects, processing, and memory.[1] In this paper we describe schemes for realizing an optoelectronic interconnection stage for optical computing and switching applications along with a quantitative analysis of system performance and device parameters. Such an interconnection scheme will also be attractive for parallel interconnection of silicon VLSI processors.

An important prototype for a photonic interconnection system is the shuffle network.[2-4] The essential feature of this system (Fig. 1) is the spatial interconnection of pixels. While large scale spatial interconnection is difficult to accomplish by conventional electronic means at high frequencies (>1 GHz), optical signals with their properties of noninterference in a homogenous medium and raylike nature are the ideal means to do so.

Computing involves not only the interconnection but also the processing of signals according to desired algorithms. The archetype processing element of conventional electronics is the three-terminal device which can function either as a linear amplifier or as a logic stage. Its most important property is the ability to give signal power gain and output fanout such that interconnections with several subsequent logic stages can be established. Similarly, the archetype processing element for all-optical processing is the three-terminal photonic device, capable of performing functions analogous to its electronic counterpart. Unfortunately, such an all-optical device having a gain or processing efficiency comparable to electronic devices has not yet been demonstrated.

Thus, the optoelectronic approach can offer the right blend of photonics and electronics for both optical computing and interconnection. A generic optoelectronic processing structure is shown in Fig. 2. In this scheme, interconnection between the processing stages is carried out optically. A detector converts the input light signals into proportional electrical signals, which are then amplified and processed using conventional electronics. The processed signals are subsequently used to modulate an optical transmitter which produces the optical output of the stage. A typical interconnection would consist of an array of pixels, each having the same schematic structure as in Fig. 2, which allows for the implementation of control. In a computer architecture, these stages also need to provide the necessary fanout of the signals to subsequent stages. The realization of large scale electronic networks using the architectures shown in Figs. 1 and 2 are still beset by numerous problems such as difficulty in

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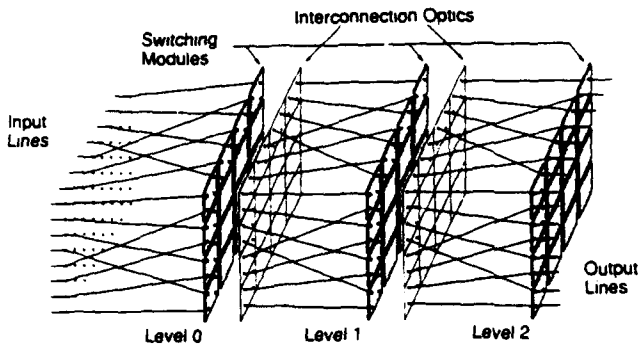

Fig. 1. Schematic of an optical implementation of a shuffle interconnection network (after Sawchuk and Glaser[4]).

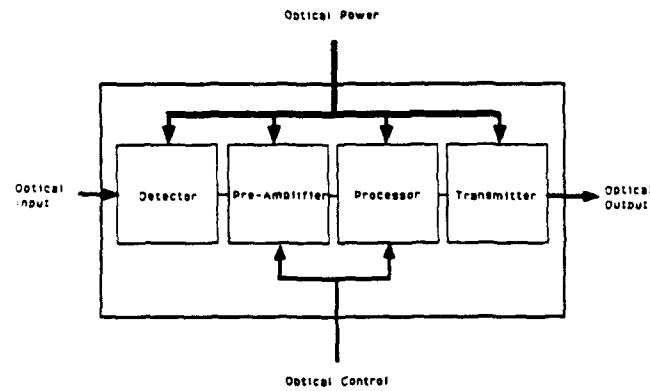

Fig. 2. Generic optically powered and controlled optoelectronic structure for optical computing and interconnection.

interconnection, high frequency parasitic coupling between elements, excessive power dissipation, etc. In the systems discussed in this paper we overcome several of these difficulties by using a novel architecture where both control and power to the pixel is supplied by optical means, as opposed to electronically supplied power used in conventional systems. This approach underlines the essential advantage of optoelectronics: It uses reliable, high performance electronic technology for processing the signals, while utilizing the advantages of photonics for the interconnects.

Recently, the concept of optical powering has attracted renewed attention. The idea was first proposed and demonstrated for communications,[5–7] and recently, for an optical interconnection system.[8] The latter work provides the archetype for this study. The use of optical powering to achieve an all-optical optoelectronic system has many potential advantages. Parasitic reactances due to power supply lines in extensive 2-D arrays can be reduced, hence reducing interchannel crosstalk. Further remote control of interconnections is made possible by implementing the control signals optically. In applications where the constraints on supplying power through wires and high, optical powering offers a simple way to access modules. It can be realized by incorporating dedicated photovoltaic cells into each of the processing pixels (Fig. 3).

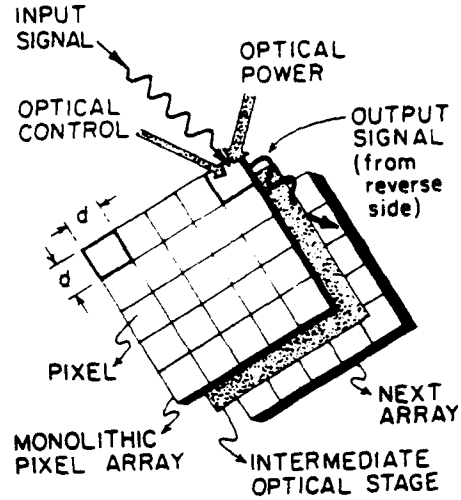

Fig. 3. Realization of optically powered and controlled interconnection array.

Power is incident on the structure through a separate light beam, which is distributed appropriately to each pixel.

This paper, which considers in detail the advantages and limitations of the optically powered optoelectronic approach, is organized as follows: In Sec. II we discuss two circuit schemes for use in the arrays. Also, we describe the use of optical powering as well as schemes for optical control. In Sec. III we quantitatively show that optical powering is a means to realize high bandwidth optoelectronic structures. In Secs. IV–VI we quantitatively discuss the circuit schemes of Sec. II with respect to gain and power dissipation. Design curves for different device technologies are derived, and the relevant trade-offs are determined. Both bipolar and field effect transistors made from $In_{0.53}Ga_{0.47}As$, InP, and GaAs are compared in terms of their power dissipation performance. We conclude in Sec. VII with a performance comparison of optically powered optoelectronic, conventionally powered optoelectronic, and all-optical system architectures.

II. Implementation of Optically Powered and Controlled Interconnects

An archetype interconnection system consists of an array of optoelectronic pixels, each having the structure shown in Fig. 2. The array itself is optically powered by photovoltaic cells located within each pixel. The control signals are also implemented optically. Once the connection is established by the control signal, the output of the transmitter is focused by the intermediate lens stages onto a given pixel in the array of the next stage, and so on (see Fig. 1).

The transmitter stage of each pixel uses a laser diode because of its high efficiency. The type of amplifier employed depends on the method used to take the laser beyond threshold. In the first scheme [Fig. 4(a)], the laser (L) is biased just below threshold, requiring only a small signal optical input to the pixel. Small here is decided by the sensitivity of the detector (PD)

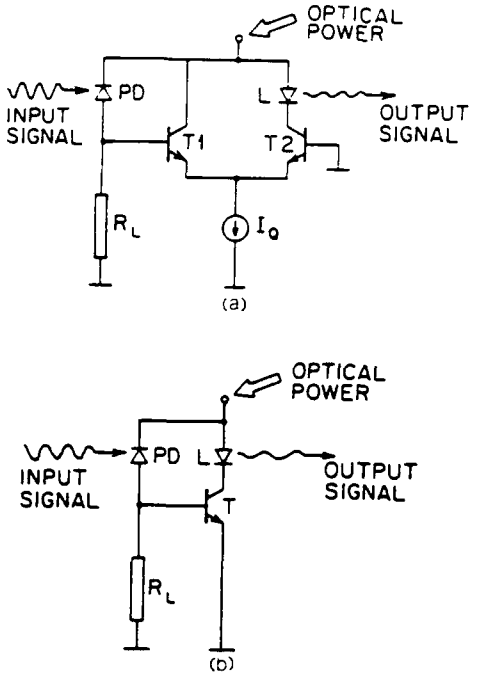

Fig. 4. (a) Schematic of a prebiased laser circuit. (b) Schematic of the unprebiased laser circuit.

and is defined as the minimum signal power necessary for the signal to be distinguishable (at a given error rate) from noise and other spurious background signals. Typically, receiver sensitivities must be greater than −25 dBm for bandwidths <1 GHz,[9] assuming a bit error rate of 10^{-12}. Thus, the input is a small signal incremental quantity. The amplified output incremental current takes the laser beyond threshold. There are several difficulties associated with this prebiased arrangement. First, the threshold current of the laser varies considerably with temperature,[10] making it difficult to control in extensive 2-D arrays such as the one shown in Fig. 3. Second, the turn on of the laser is soft due to spontaneous emission, thus requiring significant gain from the amplifier circuit. Finally, the system performance is degraded by noise at the amplifier ports,[11,12] which includes both the equilibrium as well as switching noise. In spite of these difficulties, such a prebiased system is needed in analog applications where linear response is essential, as well as in applications where the input signal level is close to the noise threshold.

The second scheme [Fig. 4(b)] is not to prebias the laser. The amplifier is turned on by the input signal, and the resulting output current takes the laser beyond threshold. This scheme has the advantages of not being seriously affected by variations in laser threshold current, or by the presence of equilibrium noise, although switching noise remains a major design problem. As noted above, however, the scheme is not suitable for small signal analog applications.

Note that both schemes benefit from the use of very low threshold lasers such as those demonstrated recently in both the AlGaAs/GaAs[13] and InP/InGaAsP[14] materials systems. We will study further the characteristics of both schemes as they apply to large 2-D arrays in the following sections.

Optical powering can be implemented using a cw beam that is divided and distributed to the array pixels using conventional lens[8] or grating stages. The number of pixels that can be powered in this manner is limited by the geometric properties of the optical stages, the coupling efficiency, and the power dissipated by the array pixels. The optics constraints arise from the size and intensity of the power beam incident on a photovoltaic (PV) cell. As a worst case, we assume that all the power incident on a pixel is dissipated as heat. Then, the maximum intensity of the beam is limited by the maximum areal power dissipation density, σ_p, permitted by the chip's cooling system. A typical value of σ_p is 1 W/cm^2.[15] In Sec. VI, we show that the typical pixel linear (d) dimension (as determined from power dissipation criteria) for circuits such as those in Figs. 4(a) and (b) is somewhat <1000 μm, suggesting that the power dissipation per pixel cannot exceed 10 mW. Thus, we can expect to have ~100 pixels/cm^2 in an optoelectronic architecture. Further, assuming the power source is a 1-W cw GaAs laser with a 50% coupling efficiency to the pixels, we conclude that a single laser can be used to power >50 pixels. If the data signal is at a wavelength of 1 μm, the geometric limits set on the pixel size by the resolution of the optics will be much weaker than the thermal one. We show that the nonideal efficiency of the PV cell leads to a further, proportionate reduction in pixel packing density (i.e. the number of pixels allowed per unit area consistent with σ_p). These considerations are discussed further in the following sections.

An advantage of optoelectronic over all-optical approaches is the ability to control the processor efficiently. The use of optical signals for control gives a versatile system that mimics all-optical ones. The implementation of the optical control of a pixel can be done via devices such as photodiodes and phototransistors incorporated into the circuit. A separate control signal is used to activate the detector or amplifier stage of the processor.[16] The choice of the point of switching depends on the amount of noise introduced by the switching process in comparison to the signal level. For example, in the prebiased laser scheme where input signal levels are small, the switching is accomplished best at the stage following the amplifier. In the realization of a hybrid optoelectronic crossbar switch, Forrest *et al.*[16] used a transistor array to switch the detector stage to the power supply. They measured switching times of 10–200 ns, these being determined by the RC time constant of the switching device–active load combination. The scheme can be controlled optically by switching the transistors with a control beam incident on standard detector stages such as PIN photodiodes.

A typical control signal distribution scheme is to modulate a control beam array by a series of acoustooptic (AO) modulators.[17] The outputs of the modulators are focused on the pixel control elements. Typi-

cally, AO modulators can be modulated at frequencies >500 MHz.[18]

III. Crosstalk

The primary source of switching noise in high frequency systems is the propagation of switching transients from one pixel to another via the power supply lines running between several closely spaced pixels. In addition, these lines are parasitically coupled by distributed reactances. This crosstalk coupling can drastically degrade the performance of electronic systems at high frequencies.[19] The conventional solution to the problem is to design suitable decoupling schemes to improve the isolation of adjacent stages. However, such decoupling is rarely adequate at high bandwidth and requires the use of large decoupling capacitors. The decoupling using optical powering is far more effective and provides for high density circuits. Optical powering can also be used for biasing symmetric self-electrooptic effect (S-SEED) based optical logic arrays. Crosstalk between long power supply lines running across these arrays can be reduced drastically, thus increasing the crosstalk-limited switching frequency.

In a large 2-D array of pixels, each element has neighbors at various distances from it. In a digital transmission scheme, the effect of crosstalk from signals incident on neighboring pixels is to change the decision levels of the system, thus leading to bit errors. In the case of asynchronous transmission, we can treat the crosstalk as additive Gaussian noise. In this case, the bit error rate (BER) is given by[11]

$$\mathrm{BER} = 1/(2\pi)^{1/2}\,[\exp(-Q^2/2)/Q], \tag{1}$$

where Q is the ratio of the root mean square (rms) signal voltage to the total rms crosstalk voltage. Crosstalk χ is defined as the reciprocal of Q. Using Eq. (1), for a BER $<10^{-12}$ the total crosstalk must be less than -17 dB.

The worst case is given by a synchronous transmission system when the signal level in the primary pixel corresponds to a zero while those at all the neighboring (secondary) pixels correspond to a one. While a statistical analysis of this situation is difficult, we can expect that the crosstalk performance of this scheme will be poorer than that of the asynchronous case. This is because it is the amplitude of the crosstalk signal that is important in the synchronous case, while the rms value of χ decides the BER in the asynchronous case.

Returning to the asynchronous case, we assume that the neighbors of a given pixel can be classified as eight first-order nearest neighbors [indicated by ones in Fig. 5(a)] and sixteen second-order neighbors twos in Fig. 5(a)]. Higher-order neighbors are neglected in comparison. Then, the total worst-case crosstalk is given by

$$\chi = 8\chi_1 + 16\chi_2, \tag{2}$$

where χ_1 and χ_2 are the rms crosstalk values due to each first- and second-order neighbor, respectively.

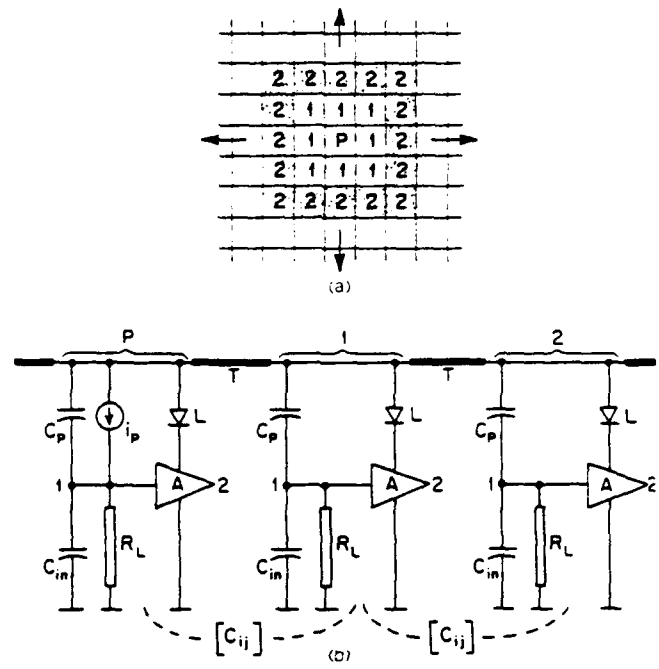

Fig. 5. (a) Schematic of the nearest neighbor approximation for a pixel in a large 2-D array. (b) A simple 1-D incremental equivalent circuit for the array in (a).

For high switching frequencies, the transmission line nature of the circuit elements becomes important and an accurate estimation of χ_1 and χ_2 requires sophisticated models.[20,21] The simplest approximation to this situation is the "lumped capacitance" model.[22] This approximation is adequate for switching times >200–300 ps and line lengths ≈1 mm.[23]

A simple 1-D incremental equivalent circuit for the array in Fig. 5(a) is shown in Fig. 5(b), which applies to the prebiased laser case. The current source, i_p, represents the primary photocurrent, A the amplifier, C_p the capacitance of the photodiode, R_L the input load resistor, and C_{in} the capacitance due to the amplifier input port and the resistor. The transmission lines represent the power supply lines in a conventionally powered case. In the optically powered case these lines are absent. As mentioned, the coupling between the pixels in the conventionally powered scheme can be reduced by introducing large decoupling capacitors between the power supply and ground. This provides a short-circuitlike path to ground for the high frequency signals on the transmission lines. Typically, such monolithic capacitors use metal insulator semiconductor (MIS) technology. Using $\epsilon_r = 4$ for the insulator dielectric constant and an insulator thickness of 1000 Å, the capacitance per unit area is 35 nF/cm^2. For a given grounding capacitance, we can thus calculate the chip area required using a MIS structure.

The conventional method of analysis[22] of crosstalk in such a circuit is to calculate the Maxwellian capacitance matrix coupling the nodes in one pixel to those in the neighbors. The matrix element C_{ij} relates the charge on node i of a given pixel to the voltage on node j

Table I. Parameters Used in Crosstalk Calculations

Symbol	Parameter	Value	Units
C_D	Photodiode capacitance	0.5	pF
C_{in}	Amplifier input capacitance	0.5	pF
d	Pixel dimension	1	mm
Z_0	Line impedance	75	Ω
W	Linewidth	5	μm

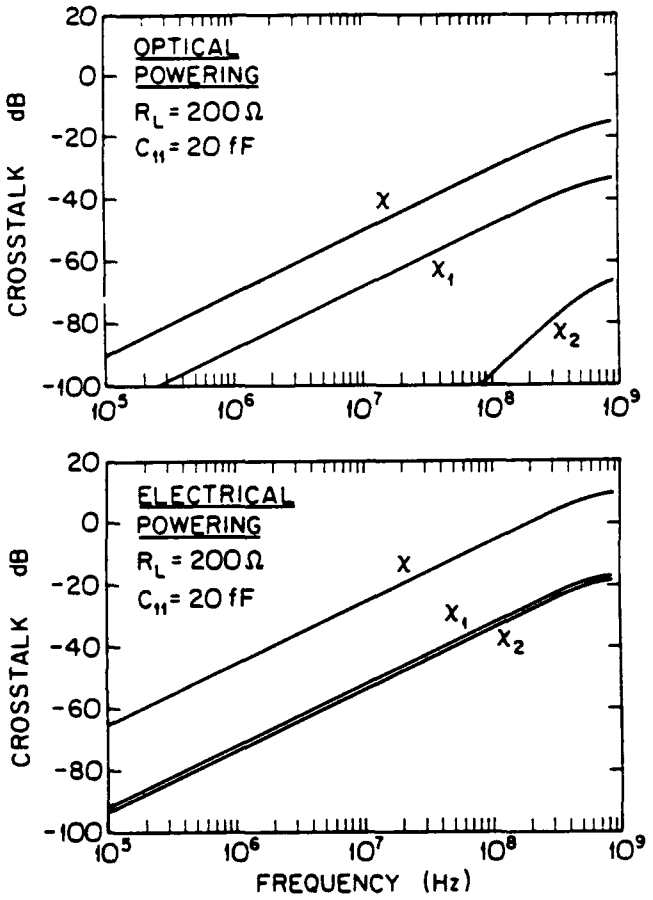

Fig. 6. Typical variation of first- (χ_1) and second- (χ_2) order crosstalk as a function of frequency for an optically (top) and electrically (bottom) powered array. The total crosstalk (χ) is also shown.

of an adjacent pixel. For simplicity, we restrict these nodes to be the input and output ports of the amplifier stage alone. Thus, the capacitance matrix in our case can be written as

$$C = \begin{matrix} C_{11} & C_{12} \\ C_{21} & C_{22}, \end{matrix} \tag{3}$$

where 1 and 2 represent the input and output ports of the amplifier, respectively. From Appendix A, where we estimate the matrix elements using a simplified geometry, it is found that the coupling capacitance is due mainly to the electrical interconnection lines within the pixels and the capacitance per unit length of coupling is only weakly dependent on the spacing between the lines for line spacings >200 μm. We assume that the length of these lines is 25% of the pixel linear dimension (≈1000 μm) in both the conventionally as well as optically powered cases.

The crosstalk in these conditions has been determined by simulating the equivalent circuit in Fig. 5(b) using SPICE along with the typical component parameters given in Table I. A plot of the total crosstalk (assuming $R_L = 200\ \Omega$) and its constituents [see Eq. (2)] is shown in Fig. 6 for both optical and electrical powering. The crosstalk is a linearly increasing function, indicating that the primary signal is being differentiated by the coupling capacitances. In the optically powered case, χ_2 is negligible compared with χ_1 over the entire frequency range considered. Hence, the total crosstalk can be taken entirely to be the result of first-order nearest neighbors. Further, the total crosstalk in the optically powered case is 20 dB lower than that in the electrical case (where χ_2 cannot be neglected). This shows that optical powering can provide good decoupling between adjacent array pixels.

For a BER $< 10^{-12}$, the requirement that $\chi < -17$ dB can be translated into a maximum allowed bandwidth using crosstalk calculations as shown in Fig. 6. This maximum bandwidth is plotted in Fig. 7 as a function of the leading coupling capacitance matrix term C_{11} for various values of the photodiode bias resistance R_L. The pixel packing density ρ corresponding to each value of C_{11} is shown on the top abscissa.

It was assumed in the case of the electrically powered system that the dimension of the grounding capacitance is half of pixel dimension d for a given packing density. Thus, the curves in the electrically powered case cut off when the grounding capacitance required to improve the bandwidth further becomes inconsistent (too large) for the particular packing density assumed. It can be readily seen that the optically powered architecture begins to show a sizable increase in bandwidth for $C_{11} < 20$ fF, whereas the electronically powered architecture does not benefit from using small capacitance front ends. Note that in both cases the bandwidth increases with increasing pixel packing density ρ. This results since, as ρ increases, the pixel linear dimension d must decrease. Since C_{11} depends on this dimension, we see that C_{11} decreases with increasing ρ, thus leading to higher bandwidth operation. However, for electrical powering, the increase in maximum bandwidth saturates at high values of ρ since the crosstalk in these cases becomes dominated by parasitics associated with the power supply lines. For $C_{11} \sim 10$ fF in the optically powered case, the bandwidth increases rapidly because the total crosstalk as a function of frequency begins to saturate at a value less than <-17 dB. Thus, for the given BER, the bandwidth is no longer crosstalk limited.

In both schemes, the maximum bandwidth is approximately inversely proportional to R_L. Thus, it would seem best to use a low value of R_L to minimize crosstalk. However, we show in the next section that this indirectly leads to a higher pixel power dissipation (since more gain is required from the amplifier as R_L decreases) and hence a smaller packing density. Furthermore, increasing R_L lowers the bandwidth of the

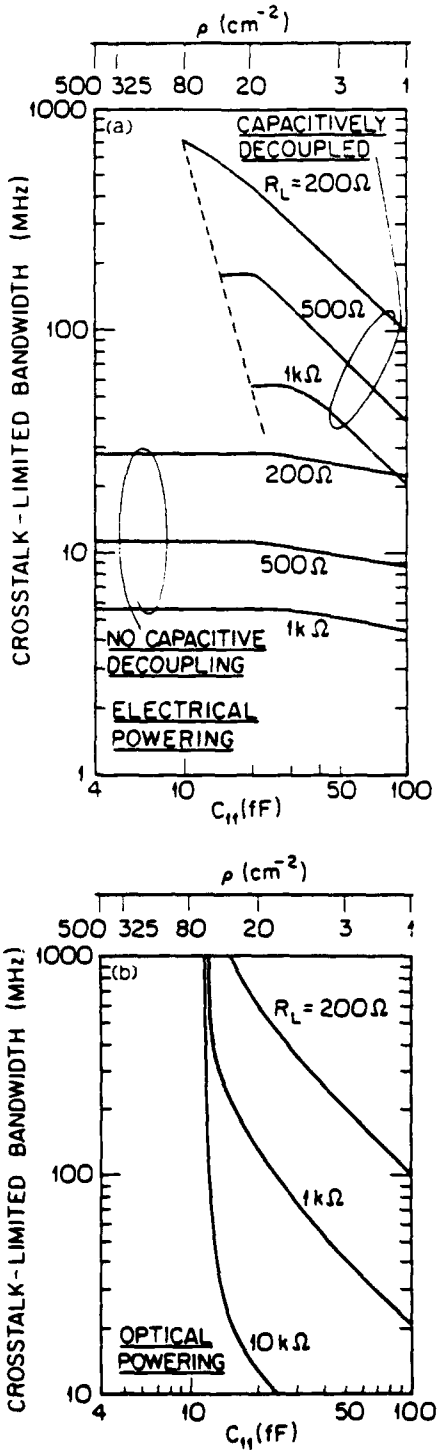

Fig. 7. (a) Crosstalk-limited bandwidth of a conventionally powered optoelectronic array as a function of crosstalk coupling capacitance and load resistance. Packing density ρ is also shown. (b) Crosstalk-limited bandwidth of an optically powered optoelectronic system as a function of crosstalk coupling capacitance and load resistance.

circuit. Hence, the optimum value of R_L is determined from a trade-off between crosstalk and bandwidth (tending to decrease R_L) and power dissipation (leading to an increase in R_L).

IV. Prebiased Laser Configuration

Consider the circuit for a prebiased pixel shown in Fig. 4(a). The photocurrent of the detector is given by

$$i_p = (q\eta_D/h\nu)P_{inc}, \tag{4}$$

where P_{inc} is the incident optical signal power, q is the electronic charge, η_D is the detector quantum efficiency, h is Planck's constant, and ν is the light frequency. The differential transistor pair, T_1 and T_2, is biased by the current source whose current is set to $2I_{th}$, where I_{th} is the threshold current of laser diode L. The output current takes the laser beyond threshold, producing the required signal power. The analysis of the scheme begins by assuming that the incident signal power is greater than the receiver sensitivity. Then, the incremental input voltage (V_s) to the differential pair is calculated by including all the parasitic and loading effects. Defining g_m as the small signal ac transconductance of the transistors in the differential pair, the output incremental current is given by

$$i_0 = g_m V_s/2. \tag{5}$$

If we define the conversion efficiency of the laser as V_c, the power incident on a pixel in the next array stage is

$$P_N = \eta_c V_c g_m V_s/2F, \tag{6}$$

where η_c is the interconnection optics efficiency. Here, a fanout of F corresponds to an equal distribution of the output power of the laser to F subsequent pixels. To ensure complete regeneration of the signal at each interconnection stage, we require $P_N \geq P_{inc}$. Thus,

$$g_m \geq 2(F/\eta_c)(P_{inc}/V_s V_c). \tag{7}$$

Now, V_s/P_{inc} is the transfer impedance $Z(f)$ of the photodiode–load resistor combination. Given $V_f = h\nu/q\eta_D$, then

$$g_m \geq 2(F/\eta_c)(V_f/V_c)[1/Z(f)]. \tag{8}$$

For a wavelength of 1.35 μm, a detector quantum efficiency of 90%, and a laser conversion efficiency of 0.5 W/A, then $V_f/V_c \sim 2$. Thus, we require g_m to be at least $4/Z(f)$. Further, since $Z(f)$ (which is a function of R_L) has a low pass behavior, the required transistor transconductance [Eq. (8)] increases with frequency. Figure 8 shows the minimum required transconductance as a function of the effective fanout, $F_{eff} = F/\eta_c$, for $C_p = 0.5\ pF$, and $R_L = 1\ k\Omega$ and 200 Ω (other parameters used in the calculation are given in Table I). Typically, values for V_c for InGaAsP/InP-based lasers are <0.4 W/A per facet.[24] and 0.5 W/A for GaAs/GaAlAs-based lasers.[25] From these results we conclude that receiver transconductances of at least 4 mS are needed to obtain $F_{eff} \geq 1$, assuming $R_L = 1\ k\Omega$. Note that, for $R_L = 200\ \Omega$, nearly five times higher g_m is required to achieve the same F_{eff}. Thus, although the maximum bandwidth achieved is higher for lower values of R_L, the requirement for higher g_m implies a concomitant increase in both pixel size and power dissipation—both factors leading to a lower ultimate packing density ρ.

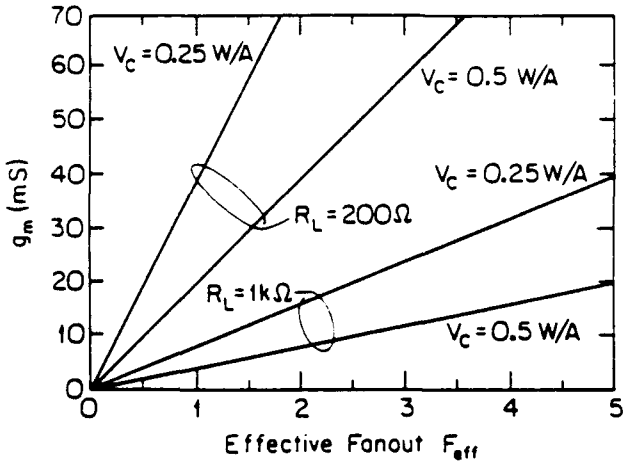

Fig. 8. Minimum transconductance required of each transistor in the prebiased laser scheme [Fig. 4(a)] as a function of the effective output fanout and load resistance R_L. The conversion efficiency of V_c = 0.5 V corresponds to reported high values in InGaAsP lasers.[3]

The usefulness of the interconnection array is decided by its total bandwidth, defined as the bandwidth of each pixel multiplied by the total number of such pixels. For a given chip area, this is accomplished by maximizing the pixel packing density ρ. Here, we estimate typical packing densities based on limitations placed on pixel size by both device and photovoltaic cell dimensions.

One of the factors limiting the pixel packing density is the amount of thermal power that the cooling system of the chip can remove. If the maximum areal power dissipation allowed on the chip is σ_p, maximum packing density ρ is given by σ_p/P_d. Here, P_d is the total power dissipated by each pixel and is the sum of the power dissipated by the amplifier, the laser, the detector, and the photovoltaic cells. For the small signal applications considered, the detector power dissipation can be neglected. The power dissipated by a transistor operating in small signal conditions is related to its dc transconductance by parameter ξ via $P_d = \xi g_m$.[26] In Appendix B we show that for a field-effect transistor (FET) $\xi = 1/2\ V_p V_{DS}$ and for a bipolar transistor $\xi = V_T V_{CE}$. Here, V_p and V_{DS} are the FET pinch off and drain source quiescent voltages, respectively. Also, $V_T = kT/q$ (where k is the Boltzmann constant and T is the ambient temperature), and V_{CE} is the output quiescent voltage of the bipolar transistor. Typically $V_p \approx 1$ V,[26] while at room temperature, V_T = 25 mV. Thus, for the same output voltages V_{DS} and V_{CE}, the dissipation of a bipolar transistor is much less than that of a FET for the same transconductance.

Let the power dissipated by the bias circuit be P_b and that of the laser be P_L. Then,

$$P_d = 2\xi g_m + P_b + P_L, \tag{9}$$

where the factor of 2 is due to the differential pair. This power is supplied by the optical beam incident on the photovoltaic cell. If the cell has a conversion efficiency of η_s, the total power input to the pixel must be

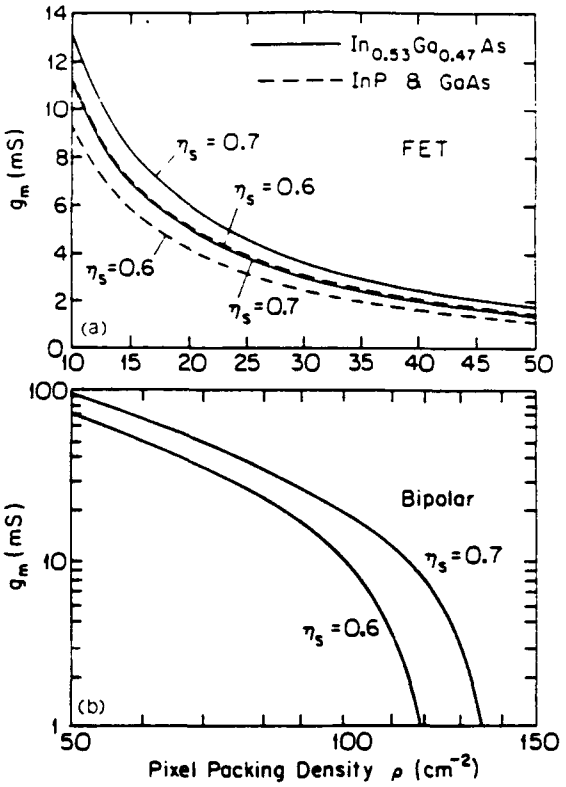

Fig. 9. (a) Maximum transconductance allowed for each field effect transistor in the differential pair of Fig. 4(a). Calculations for photovoltaic cell efficiencies of 0.6 and 0.7 are shown. (b) Maximum transconductance allowed for each bipolar transistor in the differential pair of Fig. 4(a) based on a power dissipation density of 1 W/cm.[2]

P_d/η_s. Since the input and output optical signal powers are negligible compared with the circuit dissipation, most of the input power can be assumed to be dissipated as heat. Thus, the maximum pixel packing density allowed is $<\sigma_p\eta_s/P_d$. Along with Eq. (9), this sets an upper limit on the dc transconductance of each transistor in the differential pair of

$$g_m \le (\sigma_p\eta_s/\rho - P_b - P_L)/2\xi. \tag{10}$$

As before, we assume $\sigma_p \le 1$ W/cm^2. Junction FETs (JFETs) made from $In_{0.53}Ga_{0.47}As$ with a gate length of 1 μm have ξ = 2.5 W/S,[26] while similar InP and GaAs JFETs have ξ = 3 W/S. The power dissipated by the laser diode is approximately given by $V_L I_{th}$, where V_L is the forward voltage across the laser. Laser diodes fabricated using InGaAsP-based materials show a substantially greater dissipation than GaAs-based lasers due to the presence of nonradiative Auger carrier recombination and other effects.[27,28] However, as far as the power dissipation density is concerned, this is of importance only when the optical power output of the laser is of the same order as its power dissipation. For our calculations we assume V_L = 1 V which is consistent with reported values for InGaAsP lasers.[29,30] In Fig. 9(a), the maximum g_m allowed according to Eq. (10) is plotted vs the pixel packing density for the cases of $In_{0.53}Ga_{0.47}As$, GaAs, and InP FETs.[26] Figure 9(b)

shows the same calculation for bipolar transistors, using our estimation for ξ in Appendix B.

The curves in Figs. 8 and 9 provide a method for determining the trade-offs between power dissipation and fanout. For example, for $F_{\text{eff}} = 1$, the corresponding minimum g_m for a system operating at a frequency of 1 GHz using a laser with a slope efficiency of $V_c = 0.5$ W/A and a photodiode bias resistance of 1 kΩ is 4 mS, from Fig. 8. Transferring this value to the power constraint of Fig. 9(a) (and assuming that the dc and ac transconductances are the same as 1 GHz), the maximum pixel packing density allowed using $In_{0.53}Ga_{0.47}As$ FETs is 27 cm^{-2} with $\eta_s = 0.7$. The curves can also indicate when a design is not feasible—i.e., when the minimum g_m dictated by the F_{eff} needed in a system is higher than the maximum g_m allowed from a power dissipation standpoint.

Comparing Figs. 9(a) and (b), we see that bipolar devices give much higher pixel packing densities than FETs. For the same minimum required value of g_m = 4 mS, a bipolar transistor circuit gives a packing density of 130 cm^{-2}—a value approximately five times higher than that achieved using FET circuits. Thus, bipolar transistors are clearly superior for small signal applications. Also, $In_{0.53}Ga_{0.47}As$-based FETs show a 20% lower power dissipation compared with InP- and GaAs-based ones.

V. Unprebiased Laser Configuration

In the unprebiased laser case [Fig. 4(b)], the lower limit on the signal power is determined by the turn on condition for the transistors used. In modeling the circuit, the photodiode was represented as an ideal current source, and the laser diode was assumed to have a piecewise linear transfer characteristic, while its modulation characteristics were ignored.[31]

If the input optical signal power is sufficient to turn the transistor on, the minimum current gain of the transistor must ensure that the laser will go beyond threshold. For a given P_{inc}, this nonlinear current gain is $I_{\text{th}}V_c/P_{\text{inc}}$. Further, for an effective fanout of F_{eff}, the minimum current gain K required is therefore

$$K \geq (V_l/V_c)(F_{\text{eff}} + I_{\text{th}}V_c/P_{\text{inc}}). \tag{11}$$

To evaluate the power dissipated per pixel, we let the supply voltage be V_B. Then, the mean input electrical power to the pixel is

$$P_i = V_B K i_p/2 \tag{12}$$

for a duty cycle of 50%, which is typical for many digital and analog systems. The mean output power is thus

$$P_0 = V_c(Ki_p - I_{\text{th}})/2. \tag{13}$$

The net power dissipated by the transistor and the laser diode is the difference between Eqs. (12) and (13). Adding the power dissipated in the detector (P_{det}) to this difference, we find the total power dissipated in the pixel to be

$$P_d = V_B K i_p/2 - V_c(Ki_p - I_{\text{th}})/2 + P_{\text{det}}. \tag{14}$$

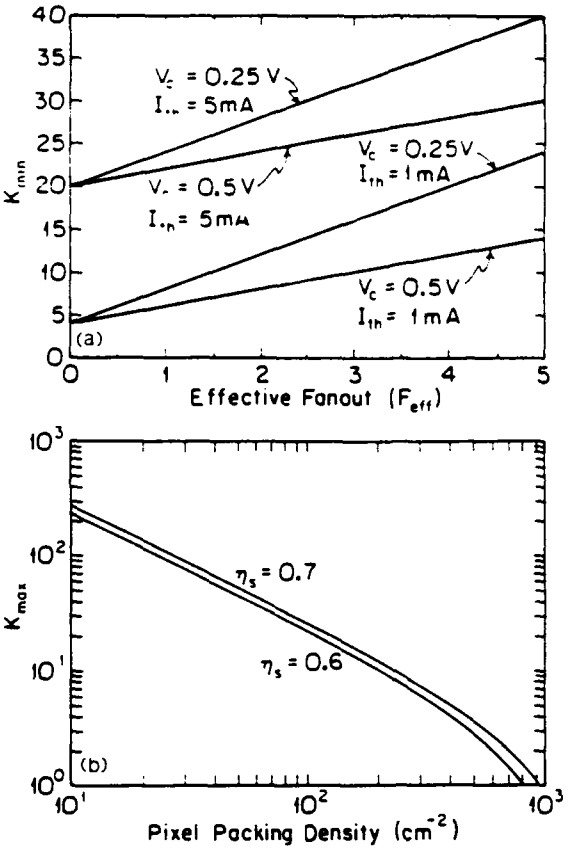

Fig. 10. (a) Minimum value of the nonlinear current gain required of the transistor in the unprebiased laser circuit as a function of the effective fanout. (b) Maximum value of the transistor current gain in the unprebiased circuit as a function of pixel packing density.

We assume that all the incident optical signal power is dissipated in the detector stage, i.e., $P_{\text{det}} = P_{\text{inc}}$. The dissipation of power by the photovoltaic cell can be accounted for, as before (Sec. IV), by dividing the right-hand side of Eq. (14) by η_s, the cell conversion efficiency. Hence, we get

$$K \leq [2V_l/(V_B - V_c)](\sigma_p\eta_s/\rho - P_{\text{inc}} - V_cI_{\text{th}}/2)/P_{\text{inc}}. \tag{15}$$

The results of these calculations are shown in Figs. 10(a) and (b), taking $R_L = 1\,k\Omega$. The curves are similar to Figs. 8 and 9 and can be used in the same way to determine the trade-offs between fanout and pixel packing density. For example, let the best available laser have $V_c = 0.5$ W/A, and $I_{\text{th}} = 1$ mA.[13,14] Also, let the optical signal power be 0.25 mW and $F_{\text{eff}} = 1$. Then from Fig. 10(a), the minimum required value of K is 6, according to Eq. (11). Transferring this to Fig. 10(b), the maxmum allowed pixel packing density for $\eta_s = 0.7$ is 330 $cm.^{-2}$ This packing density is greater than that of the prebiased bipolar circuit case by more than a factor of 2, which is expected because of the absence of quiescent dissipation in the unprebiased architecture. The unprebiased scheme is also simpler to fabricate than the prebiased circuit, and is more tolerant to laser diode threshold current variation since the signal can compensate for the increased re-

Table II. Performance Comparison Between System Architectures

Performance parameter	Optically powered and controlled optoelectronics	Conventional optoelectronics	All-optical
Crosstalk	Low	High	Low
Crosstalk source	Capacitive	Capacitive + inductive	Optical + diffusion
Bandwidth (GHz)	1–10 GHz	<1 GHz	>10
Reconfig. time	1 ns	1 ns	100 ns
On/off contrast ratio	1000:1	1000:1	10:1
Gain/stage	1–100	1–100	<1
Fanout	<10	<10	1
Functionality	High	High	Low
Complexity	HIgh	High	Moderate
Pixel size (μm)	>500	>1000	5
Maximum packing density (cm^{-2})	300	80	>10,000(?)

quired output current swing resulting from an increase in temperature.

VI. Limiting Factors on Pixel Packing Density

We now consider an example design estimation to identify the factors that physically limit the pixel packing density. Let the material used be $In_{0.53}Ga_{0.47}As$, and the required effective fanout be $F_{eff} = 1$. From Sec. IV, the maximum allowed pixel packing density is ~15 pixels/cm^2 for FET-based prebiased circuits. For a 1-cm^2 square chip, each pixel would therefore have a minimum linear dimension of 0.2 cm. The maximum value of g_m for a 1-μm gate length $In_{0.53}Ga_{0.47}As$ JFET useful for receiver applications is 250 mS/mm.[26] Since the required g_m from Fig. 3(a) is 4 mS, the required gate width is ~16 μm. Similar InP JFETs have a maximum $g_m = 340$ mS/mm,[26] leading to a required gate width of ~12 μm. Thus, the gate width does not limit the pixel packing density.

We could similarly consider a bipolar structure which from Fig. 10(b) allows a maximum packing density of 330 pixels/cm^2 implying a minimum pixel side dimension of 550 μm. The diameter of a typical heterostructure bipolar transistor is 25 μm.[32] Therefore, transistor size is also not found to be a limiting factor in determining the pixel packing density.

Another limiting factor to pixel size is set by the dimensions of the photovoltaic cell. This is determined by the maximum electrical power it can deliver without burning out. A conservative estimate of this maximum power density is σ_p. In this worst case, the cell dimensions are identical to those of the pixel. This does not imply that there is no area left over for other electrical elements on the pixel besides the cell. The geometry of a pixel can be arranged to have the photovoltaic cell on the side of the chip facing the optical inputs, while the rest of the elements, including the laser, can be placed on the opposite side of the chip where they face the input stages of the pixels in the next array. The suitability of using InP substrates as wavelength demultiplexers in this regard has been discussed previously.[33] Here, the photovoltaic cell is made on the InP substrate. On the opposite side of the chip are the other elements of the pixel, which are fabricated using the smaller bandgap $In_{0.53}Ga_{0.47}As$. The demultiplexing of power and signal beams is based on InP having a bandgap energy of 1.35 eV (corresponding to a cutoff wavelength of 0.9 μm) while $In_{0.53}Ga_{0.47}As$ has a bandgap of 0.75 eV (corresponding to a cutoff wavelength of 1.65 μm). In this case, power is incident on the pixel at a wavelength of 0.8 μm (from a GaAs high power laser array[34]), and the signal is at a wavelength of 1.3 μm. The signal beam will pass through the InP photovoltaic cell, while the power beam is absorbed by the cell and is subsequently converted into electrical power. Since the wavelength of the signal is >0.95 μm (the band edge cutoff of InP), it will finally be absorbed by the detector fabricated in $In_{0.53}Ga_{0.47}As$ Substituting Eq. (10) into the expression for the pixel linear dimension $d = (A/\rho)^{1/2}$, the size of a pixel in the optically powered case increases by a factor of $1/(\eta_s)^{1/2}$. For $\eta_s = 0.7$, this corresponds only to a 20% increase in the linear dimension of a pixel.

VII. Summary and Conclusions

In Table II we present a performance comparison between system architectures based on optically powered and controlled optoelectronic systems, conventional optoelectronic systems, and all-optical schemes. The main advantages offered by the optoelectronic system over all-optical architectures currently under study are signal gain, optical control, and output fanout.

All-optical systems show much lower crosstalk than conventional optoelectronics (typically less than −15 dB) because of the absence of electrical coupling between pixels. By using optical powering, we have shown that the electrical crosstalk in optoelectronic systems can be drastically reduced; this leads to improvements in bandwidth by more than a factor of 10 when compared to conventionally powered schemes. In addition, the reduction of circuit parasitics improves the frequency performance of the detector, as well as the reconfiguration time of the control system. We have also shown that the size of the photovoltaic cell does not limit the pixel packing desnity, especially if we use InP-based structures with natural wavelength demultiplexing by substrate absorption.

It is shown in Table II that there is a large difference in pixel packing densities between optoelectronic and

all-optical systems. It has been suggested[35] that the packing density in all-optical free space interconnection systems is limited only by the resolvable spot size of the beam, and that this leads to optical interconnect densities up to 50,000/mm^2. Against this, optoelectronic systems offer packing densities <1000 cm^{-2}. This marked disparity is balanced by the advantages offered by the latter approach over the former: broadcast capability of the pixels with signal gain and fanout, digital as well as analog processing, and dynamic reconfiguration of the interconnect. One question typically unanswered in all-optical schemes is the source of light for the data signals. The input signal power in an all-optical system must be high enough to overcome attenuation at an interconnect stage. Even in applications such as telephony, the signal received from the subscriber must be amplified so as to efficiently pass through the interconnection stages. Thus, a high density laser array is needed near the pixel array input. Optical amplifiers have been proposed for this purpose, but thus far they have proved to be dissipative for monolithic applications.[36] They also show significant insertion losses and their requirement of wavelength matching demands controlled ambients,[37] all of which are not suitable for large scale integration.

Within the framework of the optically powered optoelectronic scheme, the power dissipation performance of the unprebiased circuit is better than that of the prebiased one by a factor of 2. In the prebiased structure, bipolar transistors dissipate far less than FETs for the same value of transconductance. Furthermore, $In_{0.53}Ga_{0.47}As$-based FETs show a 20% smaller power dissipation performance than InP or GaAs FETs. We have also shown that the higher transconductance of InP and GaAs FETs is not important in determining the pixel size.

On the transmitter side, InGaAsP-based lasers show greater losses than GaAs-based ones for a variety of reasons. They also show a greater temperature dependence of threshold current compared with GaAs lasers, with a T_0 of ~100 K[38] compared with 200 K for GaAs. This has different implications for both the prebiased and unprebiased structures. With regard to power dissipation, the prebiased laser circuit is unaffected by nonradiative Auger recombination effects because the output current swing, and hence the optical power output, is small. More importantly, the variation of threshold current by even a fraction of the total output swing can seriously degrade the performance of the system, thus requiring effective feedback compensation. In the unprebiased configuration, the threshold current variation with temperature is not as serious a problem as it is in the prebiased case, obviating the need for a feedback stabilized bias.

In conclusion, the optically powered and controlled unprebiased system fabricated using bipolar, wavelength demultiplexing $In_{0.53}Ga_{0.47}As/InP$ structures offers a powerful means for implementing high frequency, high density (low dissipation) optical computing, and interconnection architectures. The improvement of the laser slope efficiency, receiver frequency performance, and chip heat removal can significantly improve the overall system performance.

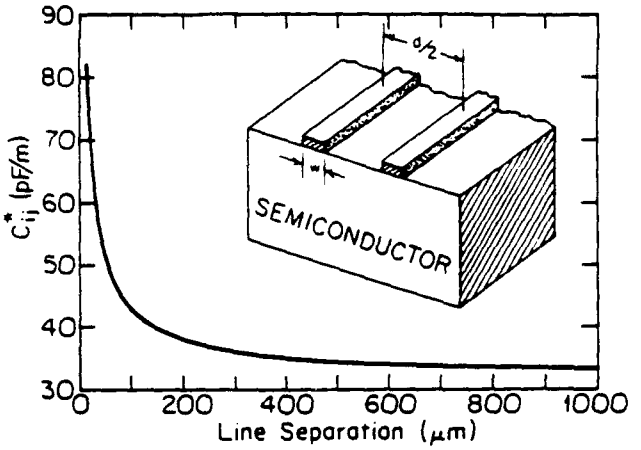

Fig. 11. Coupling capacitance per unit length calculated as a function of line spacing.

Appendix A. Estimation of the Coupling Capacitance Matrix

In their analysis of PIN photodiode arrays, Kaplan and Forrest[39] have shown that the dominant term in the coupling capacitance between adjacent array elements is a result of the fanout lines in each pixel. To calculate this effect in our case, we use a simple two-wire capacitance formula[40] where two infinite, flat strips occupy the regions $a < x < b$ and $-a > x > -b$ in the $z = 0$ plane. If the lines terminate on nodes i and j of adjacent pixels, respectively, the coupling capacitance per unit length is given by

$$C^*_{ij} = \epsilon_{\text{eff}} K(m)/K(n), \tag{A1}$$

where ϵ_{eff} is the effective permittivity of the flux linkage paths in both the semiconductor and air, K is the complete elliptic integral of the first kind, with n being defined as a/b, and $m = (1 - n^2)^{1/2}$. We also assume that $\epsilon_{\text{eff}} = (1 + \epsilon_r)/2$ where ϵ_r is the relative permittivity of the semiconductor material.[24] The average separation between the lines is $d/2$ (where d is the linear dimension of a pixel) while their width is taken to be w (see inset in Fig. 11). Then $a = 1/(1 + 4\ w/d)$. Because of the elliptic integrals, C^*_{ij} has a weak dependence on both W and d, rising to higher values only for values that are comparable to W, as shown in Fig. 11. For long lines, i.e. lines whose lengths are much greater than their widths, the capacitance for a coupling length l is given by $C^*_{ij}l$.

We further assume that the off-diagonal terms of matrix C are one-half of the diagonal terms. This takes into account the reduced coupling between off-diagonal nodes and also prevents the capacitance matrix from becoming singular, which would then leave the inductance matrix undefined.

Appendix B: Estimation of ξ

By definition,

$$\xi = V_{DS} I_{DS} / [\partial I_{DS} / \partial V_{GS}] | Q, \tag{B1}$$

where Q refers to the quiescent operating point. Here V_{DS} is the drain source voltage, I_{DS} is the drain saturation current, and V_{GS} is the gate-source voltage. For a FET, the saturation region equation is

$$I_{DS} = I_{DSS}(1 - V_{GS}/V_p)^2, \tag{B2}$$

where I_{DSS} is the drain saturation current for zero gate bias. Thus, using Eq. (B1), $\xi = 1/2V_p V_{DS}$. For a bipolar device, the active region equation is

$$I_c = I_{co}(\exp(qV_{BE}/V_T) - 1), \tag{B3}$$

where I_c and I_{co} are the collector current and collector saturation current, respectively, and V_{BE} is the base emitter voltage. Thus, $\xi = V_T V_{CE}$.

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F. A HIGH SENSITIVITY, HIGH BANDWIDTH $In_{0.53}Ga_{0.47}As/InP$ HETEROJUNCTION PHOTOTRANSISTOR

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ABSTRACT

The effects of inserting a thin, low doped InP layer into the emitter of an N-InP/p^+-$In_{0.53}Ga_{0.47}As$/n-$In_{0.53}Ga_{0.47}As$ heterojunction phototransistor have been investigated by both numerical simulation and experiments. This High-Low Emitter structure can improve both sensitivity and bandwidth over conventional structures at low input optical power by decreasing the bulk recombination current at the heterointerface. Experimental results show that the photocurrent gain is independent of the incident power at high input powers. At low input power, the gain is found to have a small power dependence, with an ideality factor of 1.25. A current gain as high as 260 is obtained at an input power of only 40 nW.

INTRODUCTION

In optical fiber communications, the optical signal diminishes with distance, and the sensitivity of a photoreceiver drops at high frequency. In order to allow for large repeater separation and high bandwidth operation, photoreceivers require high gain at low optical power. Recently, heterojunction phototransistors (HPT's) have been extensively studied [1-3] as alternatives to p-i-n detectors and avalanche photodiodes for use in photoreceivers. It is well known [1], however, that the photocurrent gain (M) of a typical heterojunction phototransistor (HPT) drops dramatically at low input optical power, thereby limiting the sensitivity of the device. This behavior is attributed to different sources of recombination currents at the emitter/base heterojunction (HJ), especially interface and surface recombination. The supression of these recombination sources, therefore, are key to the improvement of the sensitivity of HPTs.

As proposed by Kroemer [4], the bulk recombination current at the emitter/base (E/B) junction can be reduced by placing a high density of acceptor impurities at the heterointerface. This implies that, for a material with a low surface recombination velocity (such as InP/$In_{0.53}Ga_{0.47}As$ [5]), we can improve the sensitivity of HPTs by growing emitter layers with high-low doping profiles. The structure is called a High-Low Emitter (HILOE) HPT, and its cross section is shown in the inset of Fig. 1.

The HILOE structure is similar in some respects to the high-low emitter, low-high base phototransistors proposed by Chen et al. [6]. However, the sensitivity of those HPTs is not expected to show improvement over a conventional structure since the low-high base increases the recombination current at the HJ [7]. Furthermore, they fabricated this structure using GaAs/AlGaAs HPTs, where the surface recombination current in the extrinsic base region is believed to be the main source of recombination [8].

Here, both device modeling and experimental results for the HILOE-HPT are presented.

DEVICE MODELING

We have simulated the transistor operation based on the drift-diffusion model [9]. In Fig. 1, we present the values of gain (M) calculated for both HILOE (solid line) and conventional (dashed line) HPTs. Here, the doping concentrations of emitter, base and collector are $4x10^{17}$ cm^{-3}, $1x10^{18}$ cm^{-3} and $3x10^{16}$ cm^{-3}; and the layer thickness are 2 μm, 0.2 μm and 2 μm, respectively. The HILOE-HPT consists of an additional N^- InP layer (of thickness d) inserted into the emitter of a conventional device. For this calculation, we take d=500 A and a doping concentration (N_{D2}) of $1x10^{16}$ cm^{-3} for the N^- InP layer.

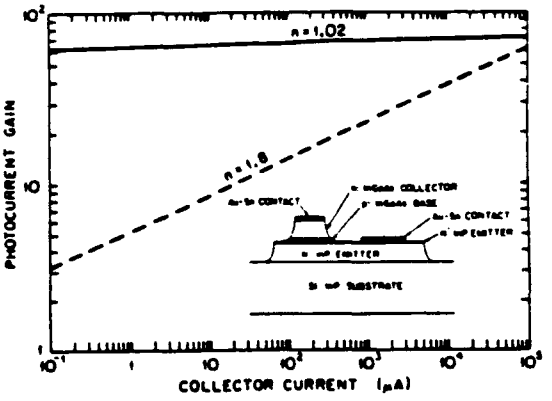

Fig.1: Calculated HILOE (solid line) and conventional (dashed line) HPT gains. Inset: Schematic cross section view of HILOE-HPT.

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As shown in the figure, the gain of the HILOE-HPT is only weakly dependent on the collector current (I_C) with n=1.02 -- an indication of diffusion current-dominated transport. On the other hand, the gain of the conventional HPT strongly depends on the collector current, with n=1.8. Hence, the HILOE structure can significantly reduce the recombination current and, in turn, enhance the gain at low input optical powers (i.e. low I_C).

The effect of layer thickness (d) and doping concentration (N_{D2}) of the low-doped emitter layer on heterojunction ideality factor (n) is shown in Fig. 2. Observe that n approaches unity by either increasing d or decreasing N_{D2} of the thin emitter layer. This implies that the recombination current can be efficiently reduced by growing a thick undoped layer into the emitter. In this case, however, large emitter series resistance degrades the frequency response of the HPT. Hence, the optimum design of layer thickness and doping concentration of the thin emitter layer is essential to obtain a combination of high sensitivity and bandwidth.

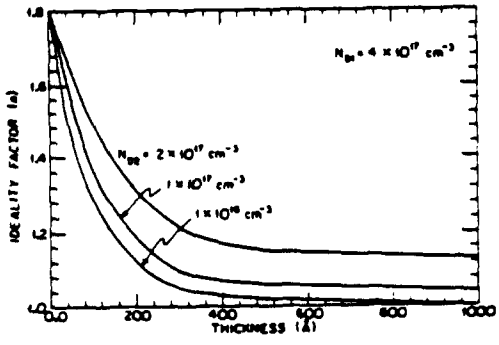


Fig. 2: Calculated heterojunction ideality factor (n) for different layer thickness (d) and doping concentration (N_{D2}) of the low-doped emitter.

The HILOE structure can reduce the E/B junction capacitance (C_E), and thus increase the bandwidth of the HPT. Furthermore, it improves the photocurrent gain at low input optical power. Hence, the gain-bandwidth product (or cutoff frequency) of HILOE-HPTs, f_T, is expected to show improvement over conventional HPTs.

In Fig. 3, f_T is calculated for different input optical powers (P_i) for both conventional and HILOE HPTs. As shown in the figure, f_T of the conventional HPT with an emitter doping concentration of $N_D=4x10^{17}$ cm^{-3} (curve 1) is small at low P_i, where the dynamic emitter resistance (inversely proportional to the product MP_i) is large, and thus limits the emitter charging time. As P_i increases, the dynamic emitter resistance decreases, and thus f_T becomes larger. Finally, f_T saturates at the power level where the total transit time across the HPT is dominated by the base and collector transit times. The response of a second conventional HPT with $N_D=1x10^{16}$ cm^{-3} (curve 2) is also shown. In this case, the enhanced photocurrent gain at low input optical power and the lower value of C_E improves f_T. On the other hand, the large series resistance of this low-doped emitter layer limits the emitter charging time, and f_T drops to 0.44 GHz at high P_i.

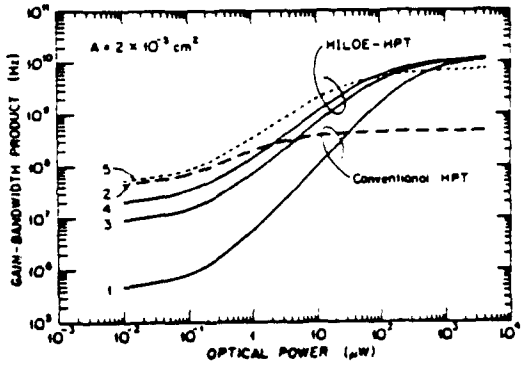


Fig. 3: Calculated gain-bandwidth products (f_T) at different input optical powers (P_i) for both conventional and HILOE-HPTs.

The gain-bandwidth product of three HILOE-HPTs with $N_{D2}=2x10^{17}$ cm^{-3}, d=0.1 μm (curve 3); $N_{D2}=1x10^{17}$ cm^{-3}, d=0.1 μm (curve 4), and $N_{D2}=1x10^{16}$ cm^{-3}, d=1 μm (curve 5) are also shown in the figure. Note that by increasing the layer thickness or decreasing the doping concentration of the low-doped emitter layer, the photocurrent gain and thus f_T is greatly improved at low input optical power. For curve 3 and 4, the emitter series resistance is small and f_T at high input power is not degraded. On the other hand, the drop of maximum f_T is clearly observed for curve 5.

EXPERIMENTAL RESULTS

The phototransistor was grown on (100) semi-insulating InP by LPE. For the HILOE-HPT (Wafer #1), 2 μm Sn-doped ($2x10^{17}$ cm^{-3}) InP followed by 0.1 μm Sn-doped ($2x10^{16}$ cm^{-3}) InP formed the emitter region. Next, a 0.2 μm, Cd-doped (~ 10^{18} cm^{-3}) base, followed by a 0.7 μm ($2x10^{16}$ cm^{-3}) collector were both grown using $In_{0.53}Ga_{0.47}As$. Wafer #2 was a conventional HPT structure.

An electrochemical profiler was used to measure the doping concentration and layer thickness of each epitaxial layer for both wafers. Fig. 4 shows the carrier concentration versus distance for Wafer #1, where a 0.1 μm ($2x10^{16}$ cm^{-3}) emitter layer is clearly observed. This InP region is n-type, implying that Sn indeed compensates the Cd diffused from the base. Furthermore, the built-in voltage at E/B junction was measured to be 0.93 eV and, in turn, the conduction band discontinuity energy (ΔE_C) of 0.22 eV was obtained. The value of our measured ΔE_C is close to the value (0.24 eV) reported in the literature [10]. As has been pointed out earlier [11], the barrier height at the E/B junction is strongly affected by the p-type dopant diffusion into the emitter. Hence, the consistency of the

measured ΔE_C with earlier data implies that Cd dopants can reduce the displacement of the p/n junction away from the HJ.

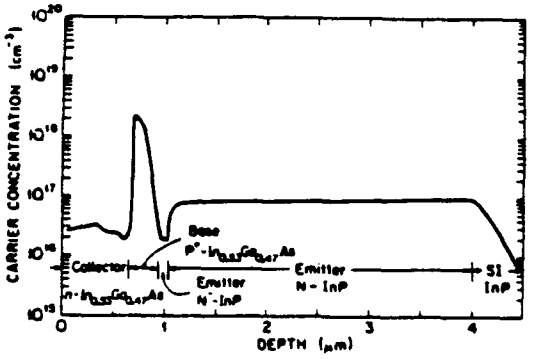


Fig. 4: Measured free carrier concentration versus distance for the HILOE-HPT.

Fig. 5 shows M (solid lines) versus I_C for both samples. The photocurrent gain of Wafer #1 is independent of I_C at high input powers, corresponding to a HJ ideality factor of n=1. At low I_C, the gain was found to have a small power dependence, with n=1.25. In contrast, the gain of Wafer #2 decreased rapidly with I_C, giving n=1.75 independent of light intensity. To our knowledge, the ideality factor of Wafer #1 is the lowest value achieved for HPTs grown using LPE.

Base contacts were formed on part of the devices on both Wafer #1 and #2. From the quantum efficiency measurement of the base/collector junction, the current gain (β) of both wafers was calculated, and the results are also shown in Fig. 5 (dashed line). Note that a high current gain of 260 was obtained at P_i=40 nW for Wafer #1, which is an improvement by a factor of 4.5 over the conventional device gain. To our knowledge, the current gain of Wafer #1 is the highest value reported in the literature for this low level of optical power.

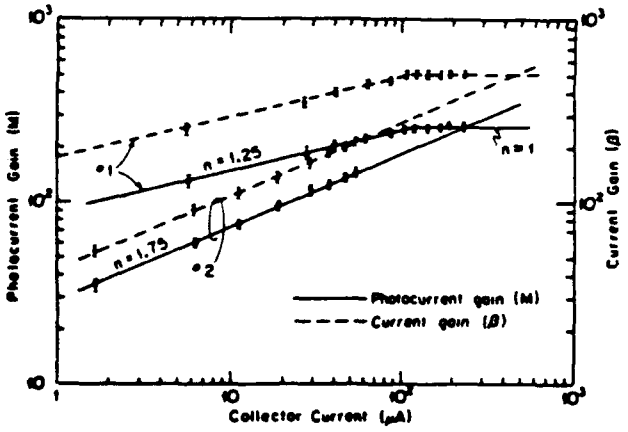
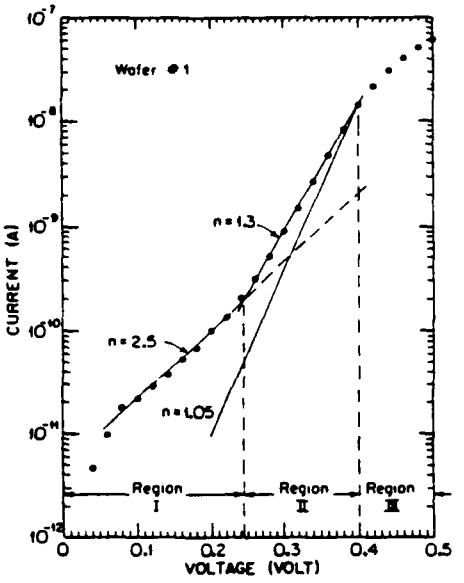
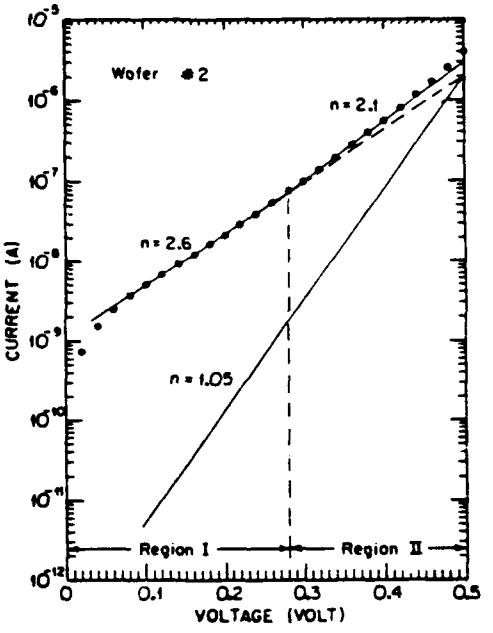


Fig. 5: Measured photocurrent gain (solid line) and current gain (dashed line) versus collector current (I_C) for both HILOE (Wafer #1) and conventional (Wafer #2) structures.

In Fig. 6(a) and (b), we compare the forward I-V characteristics of the E/B junctions for both wafers. For Wafer #1, n=2.5 at V_{BE} < 0.2 V (region I), as shown in Fig. 6(a). The large value of n indicates that base recombination current is dominant. At these voltages, the bias voltage is less than the offset voltage of the HPT, and hence this region was not accessible to the measurements shown in Fig. 5. In region II, where 0.2 V< V_{BE} < 0.4 V, the value of n (1.3) is consistent with



(a)



(b)

Fig. 6: Forward-biased I-V characteristics of the emitter/base junction for (a) Wafer #1, and (b) Wafer #2.

n=1.25 in the low-I_C region of Wafer #1 in Fig. 5. We can extract the recombination current from the *total current simply by extrapolating the current level* of region I into region II (dashed line in Fig. 6(a)). After subtracting the recombination current from the total current, the ideality factor (n=1.05) of the new curve is very close to 1, corresponding to the diffusion current. At high forward voltages, the resistance of the low-doped emitter and the lateral base resistance limit the diffusion current, causing the current to saturate in region III. Hence, the ideality factor of n=1, which corresponds to high-I_C region in Fig. 5, can not be observed in this region.

In contrast, the ideality factor of Wafer #2 is n=2.6 in region I (V_{BE} < 0.35 V), as shown in Fig. 6(b). Although the ideality factor is the same as that of Wafer #1 in region I, the recombination current is 250 times larger, and the voltage range where the recombination current dominates is also larger. In region II, n=2.1, corresponding to the low-I_C region of Wafer #2 in Fig. 5. After subtracting the recombination current from the total current, we once more obtain n=1.05.

From the above analysis, the recombination current at the HJ has been reduced by *two orders of magnitude* for the HILOE structure, and thus the HJ ideality factor is also substantially improved. This conclusion is consistent with both device modeling and the HPT photocurrent gain data in Fig. 5.

CONCLUSION

In conclusion, N-InP/p^+-$In_{0.53}Ga_{0.47}As$/n-$In_{0.53}Ga_{0.47}As$ HILOE-HPT can improve both sensitivity and bandwidth by diminishing recombination at the HJ. A current gain as high as 260 was obtained at an input power of only 40 nW. The significant gain enhancement of the HILOE-HPT indicates that both bulk and interface recombination currents at the emitter/base junction are the major sources of recombination for this material system.

The HILOE-HPT can also be applied to other material systems (such as GaAs/AlGaAs) if a proper surface passivation technique is used for reducing the high surface recombination currents. One of the strengths of the HILOE structure is that it can diminish the recombination current by reducing the minority carrier concentration in the notch region of the HJ, rather than by increasing the minority carrier lifetime. Hence, the performance of the HPTs is less dependent on the quality of heterointerface growth employed.

It has been pointed out that the use of a graded base can reduce the electron transit time [4] which decreases the base recombination current and improves the bandwidth of the bipolar transistor. Hence, the use of double emitters with a high-low carrier concentration profile along with a graded base is expected to result in both a high sensitivity and high bandwidth HPT.

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G. TuC5 Optically powered monolithically integrated logic circuits

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Optical powering of optoelectron integrated circuits (OEICs) significantly improves their performance in high density photonic systems as compared to conventional designs employing electrical powering of circuits.[1] Here optical powering replaces the dc bias lines with integrated photovoltaic (PV) cells in each pixel. The PV cell is illuminated with an external light source (e.g. laser) and converts this optical power beam into electrical power which subsequently drives the circuitry within that pixel. The total absence of the parasitic capacitances and inductances in the optical beam reduces inter-pixel cross-talk as compared with conventional dc bias lines. This leads to significantly increased bandwidths in the optically powered case. In addition, optical powering reduces interconnection complexity associated with routing bias lines to each pixel in a high-density, two dimensional array. An optically powered interconnection system has already been demonstrated in hybrid form.[2,3] In this present work, we discuss an integrated optoelectronic logic circuit in which the power and control are both provided using optical sources.

The OEIC under study is shown in Fig. 1. The circuit is optically controlled to operate as an amplifier, bistable switch/latch, or SR flip-flop. The optical power is provided using an InP PV cell illuminated with a 0.82 μm laser diode. The PV cell is sectioned into a four segment array to provide an open circuit voltage of 3.8 V. A photograph of the sectioned PV cell is shown in the inset of Fig. 2. The input data signal, transmitted by a 1.3 μm laser diode, is detected and amplified by an InGaAs/InP heterojunction phototransistor (Q_{in}). The output data signal is emitted by a 1.3 μm laser diode (LD) which is not integrated in the present circuit. Positive feedback is needed to drive the circuit into the bistable switch/latch mode, and is achieved by coupling a small percentage of the output signal onto an additional heterojunction phototransistor (Q_{fb}). The magnitude of positive feedback, which determines the optical bistability, is controlled by a second, 0.82 μm control beam incident on an integrated InP photoconductor, PC_1. Here PC_1 is 50 μm^2 and in a standard interdigitated electrode configuration with finger spacing and widths of 2 μm. The second photoconductor, PC_2, is the reset switch for the SR flip-flop. The heterojunction bipolar transistor (Q_{pb}) provides the option of applying a pre-bias to the laser diode, LD. The quiescent operating point of the circuit is set by a thin film NiCr resistor (R_L). All components, excluding the laser diode, are integrated. The integrated circuit requires growth of five epitaxial layers (Fig. 2). This structure is grown by liquid phase epitaxy on a (100) oriented InP semi-insulating substrate.

We have performed experiments to demonstrate the amplifier and bistable switch/latch modes of operation. Optical gains of 10 are achieved. The amplifiers have a sharp turn on the strong optical signal saturation (Fig. 3a). The optical feedback circuit is tuned using a 3 dB coupler from the laser output to achieve latching (Fig. 3b). The bandwidth of the heterojunction phototransistor is measured at 37 MHz and PC_1 has a bandwidth of 350 MHz with a gain-quantum efficiency product of 10.

In conclusion, we have demonstrated that optical power and control, combined with the functionality provided by electronics is a powerful means to achieve high performance, high bandwidth optical interconnects.

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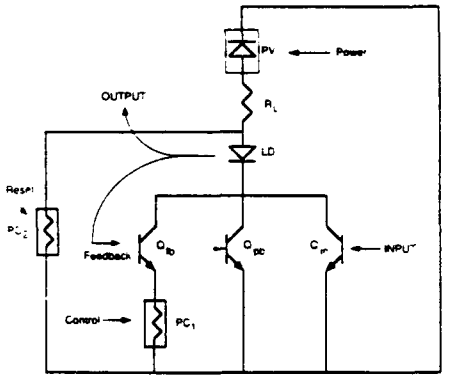

Fig. 1. Optically powered optoelectronic integrated logic circuit which operates as an amplifier, bistable switch/latch, or SR flip-flop. Optical input and control beams are at 1.3 μm (solid arrows) and 0.82 μm (dashed arrows).

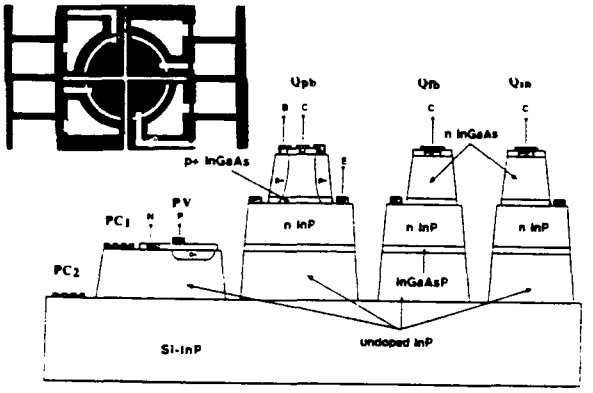

Fig. 2. Cross section of five layer epitaxial structure for circuit shown in Fig. 1. Photograph of fabricated photovoltaic cell shown in inset.

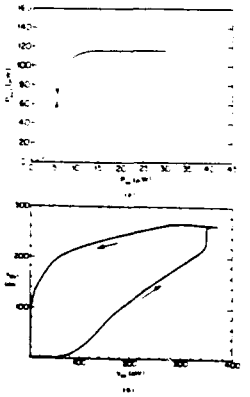

Fig. 3. Experimental results of integrated logic circuit operated in (a) amplifier mode and (b) bistable switch/latch mode with optical gain of 10.

9:00am (Invited)

H. ThH2 Optically powered smart pixels

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Recently, there is an increasing interest in smart pixel arrays for use in high density, high bandwidth interconnection networks.[1-3] Optoelectronic integrated circuits (OEICs) are attractive components for such arrays. There are, however, critical limitations associated with 2-D chip architectures that prevent the OEIC-based design from achieving the expected high performance. One issue is the electrical voltage supply and pixel logic control lines which must be routed to each pixel. The nonzero impedance of these interconnects introduces crosstalk which ultimately limits the bandwidth of the system. In addition, the dc bias lines and their associated ac decoupling circuitry consume valuable chip area. We propose a novel interconnection architecture to confront the issues of crosstalk and layout, which utilizes the principle of optically powered smart pixels.[3] Here, optical powering is locally provided to each pixel using an integrated photovoltaic cell. In this paper, we demonstrate an optically powered, integrated smart pixel. The InP based circuit can be dynamically tuned with an optical control beam to operate as an amplifier, bistable switch or as a latch/reset. The circuit has an optoelectronic gain of 2.5–11, and operates at 80 Mbit/s with an optical switching energy of only 3.8 pJ.

The fundamental limits confronting such optically powered smart pixels are discussed.

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